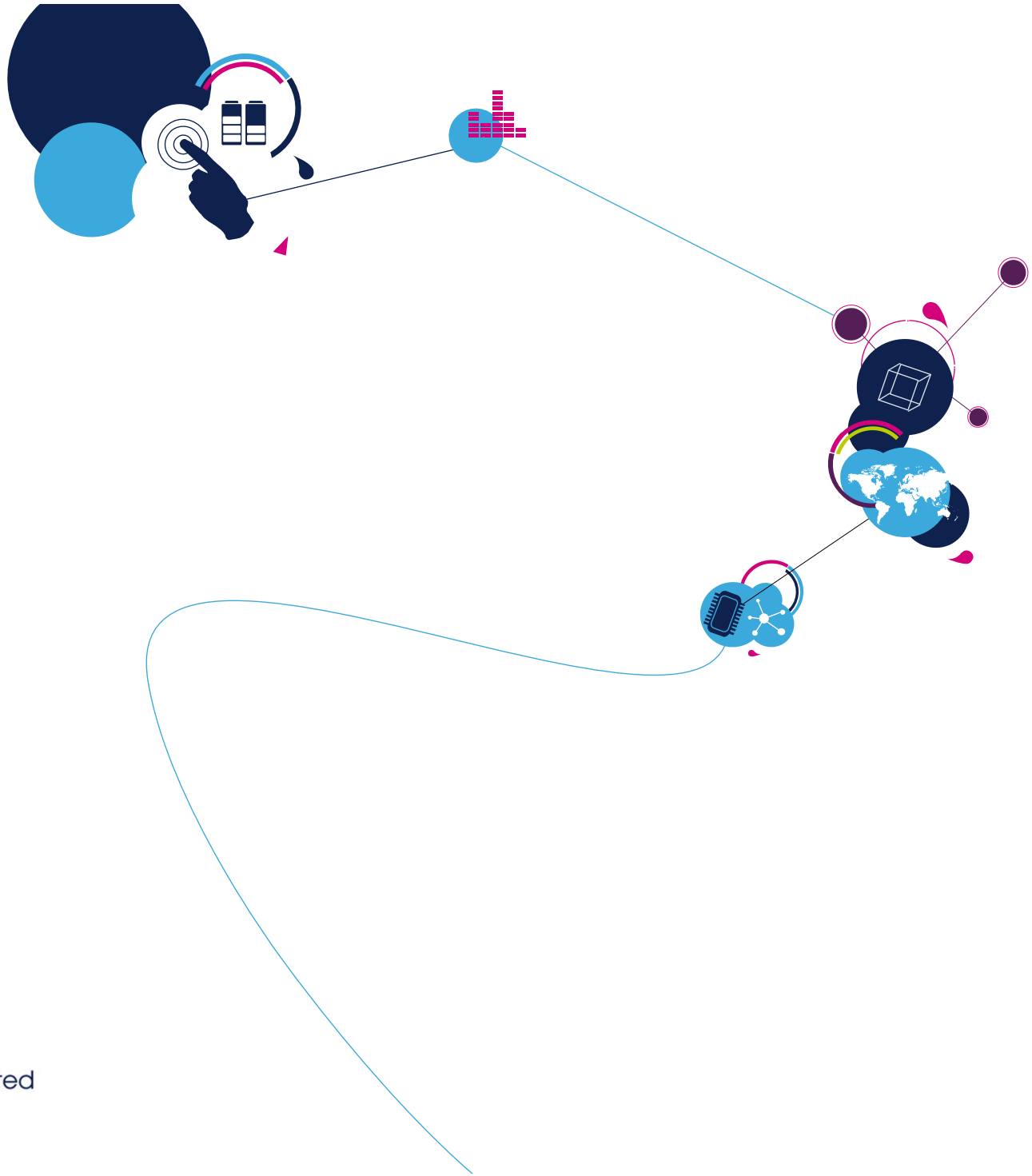

Timers

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Foreword

- At the sole exception of the LPTIMER, all STM32 timers are derived from the very same architecture
  - Same operating principle
  - Same programming registers
- Several derivatives existing with decreasing number of features
  - Advanced-control
  - General-purpose (4, 2 or 1 channel)
  - Basic
- The Low-Power LPTIMER architecture changed because of the following characteristics:
  - It offer the bare minimum features (and thus lowest possible consumption)
  - It is able to work independently from the rest of the system, typically when the MCU is in STOP mode (internal clocks disabled)
    - Ultra low-power asynchronous design

STM32 timers basic concepts

- Based on a counter with an auto-reload mechanism
  - Counting period can be directly programmed in a register All channels, when mapped to an I/O
    - No free-running timer management issues
- All channels connected to an I/O can be configured either as an input (capture) or an output (compare or PWM)
- Beside basic operation, most timers are including extra features:
  - Digital filter to remove glitches on inputs
  - PWM input mode
  - Quadrature Encoder reading or Hall-sensor mode
  - Power-conversion specifics (deadtime, current-mode management,…)
- The timers can be chained for synchronization and complex waveform management purposes

STM32L4 Timer features overview

	Counter resolution	Counter Type	PWM Mode	DMA	Capture Compare channels	Synchronization	
						Master	Slave
Advanced Control **TIM1 and TIM8**	16 bit	Up/Down	Standard + combined + asymmetric	YES	6	YES	YES
General purpose **TIM2 and TIM5**	32 bit	Up/Down	Standard + combined + asymmetric	YES	4	YES	YES
General purpose **TIM3 and TIM4**	16 bit	Up/Down	Standard + combined + asymmetric	YES	4	YES	YES
General purpose **TIM15**	16 bit	Up	Standard + combined	NO	2	YES	YES
General purpose **TIM16 and TIM17**	16 bit	Up	Standard	NO	1	YES(1)	NO
Basic **TIM6 and TIM7**	16 bit	Up	Standard	YES	0	YES	NO

(1) TIM16 and TIM17 have no TRGO output, OC output is used instead

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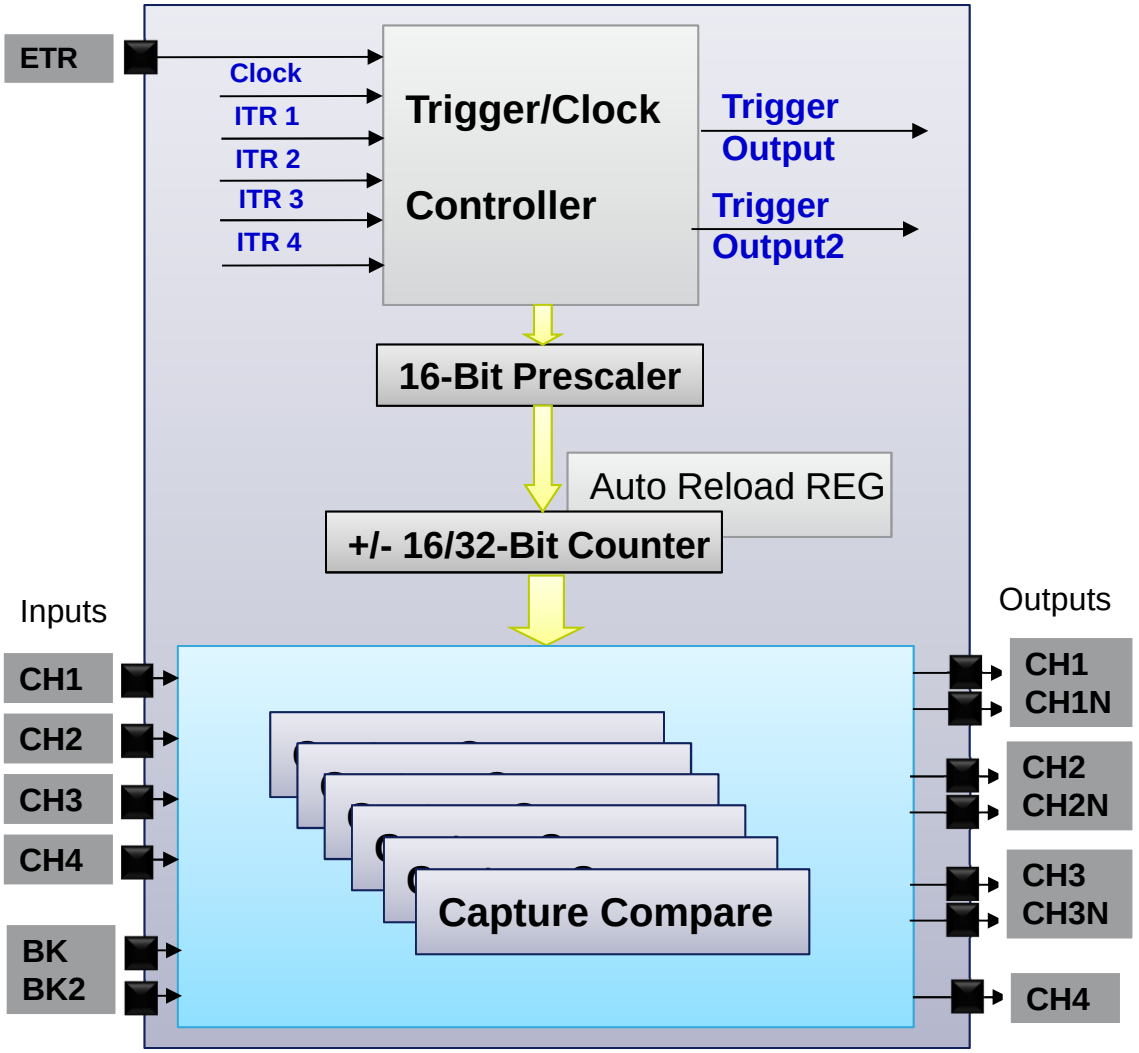
TIM1/8 TIM2/3/4/5 TIM15 TIM16/17 TIM6/7

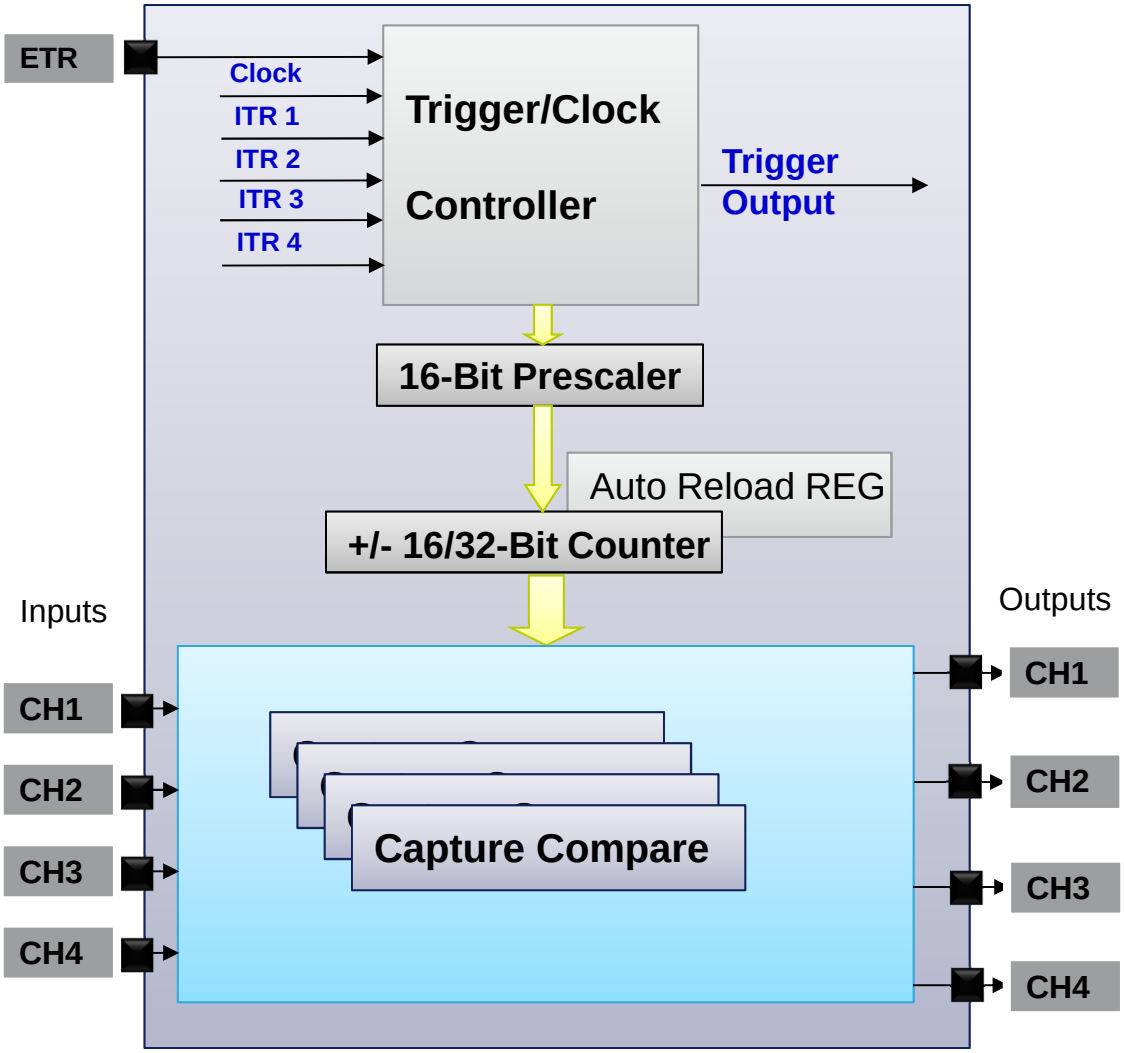
Advanced control timer

- Up to 6 16-bit resolution Capture Compare channels
- 7 outputs and 7 inputs
- Inter-timers synchronization
  - 2x TRGO outputs for additional ADC triggering options
- Up to 6 IT/DMA Requests
- Encoder Interface
- Hall sensor Interface



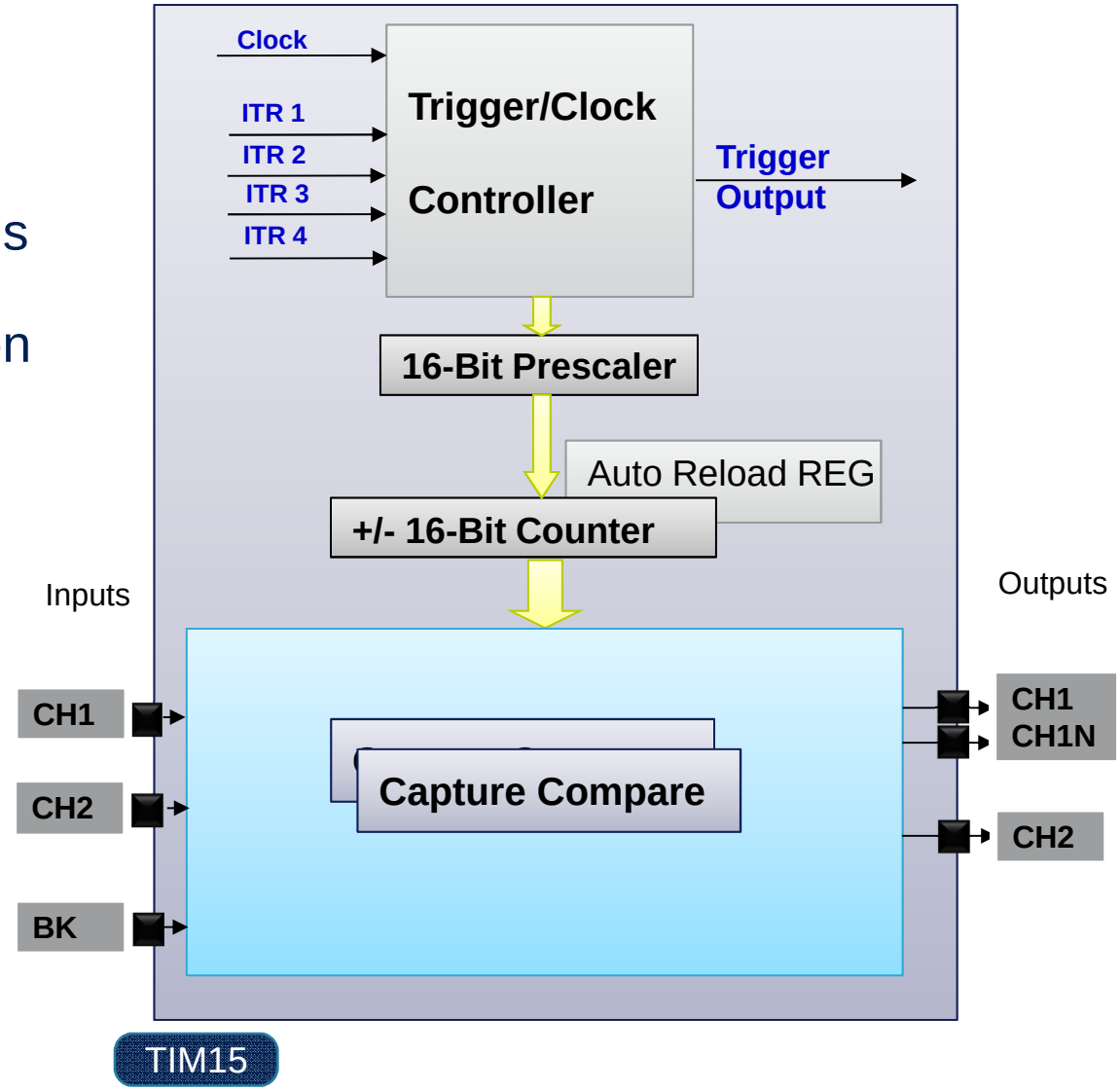
General purpose timer 4 channels

- Up to 4 16-bit resolution Capture Compare channels (TIM3/4)
- Up to 4 32-bit resolution Capture Compare channels (TIM2/5)
- Inter-timers synchronization
- Up to 6 IT/DMA Requests
- Encoder Interface
- Hall sensor Interface



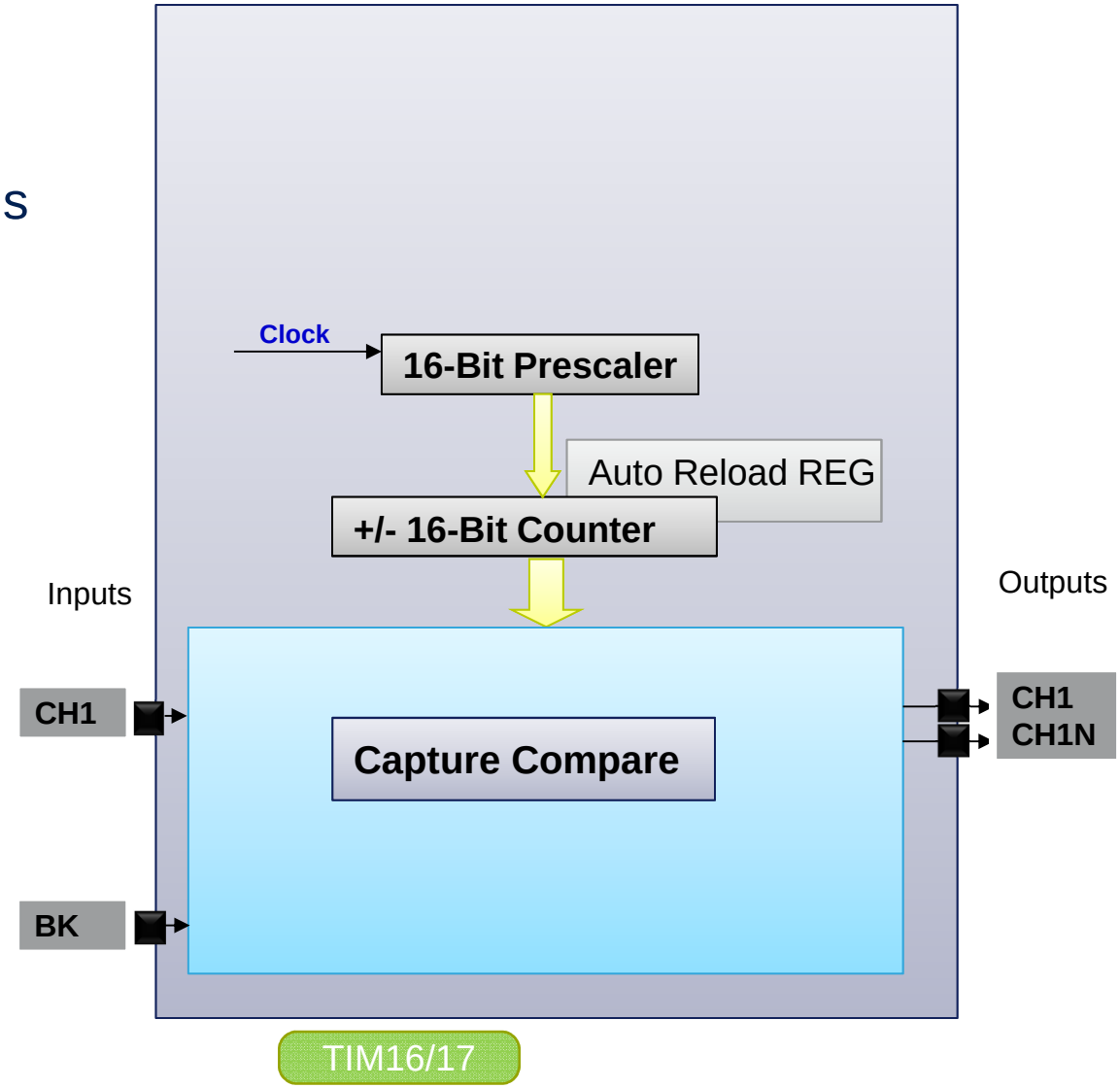
General purpose timer 2 channels

- Up to 2 16-bit resolution Capture Compare channels
- Inter-timers synchronization
- Complementary output on channel1 and channel 2



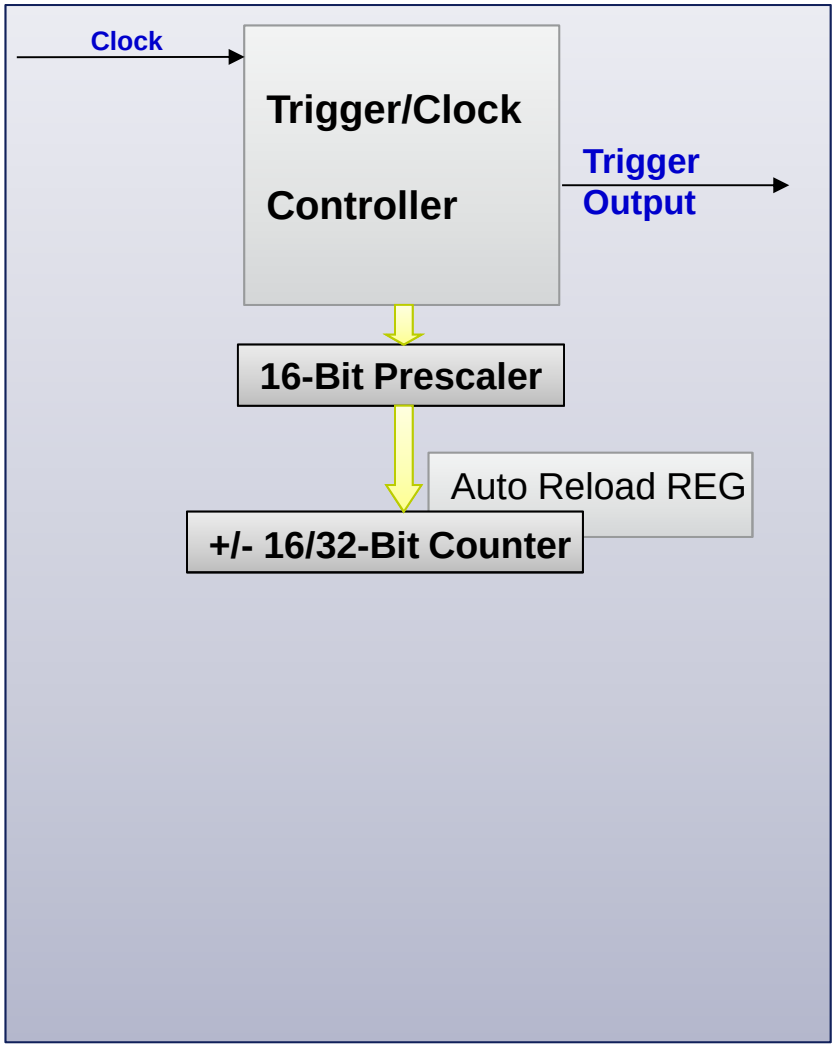
General purpose timer 1 channel

- One 16-bit resolution Capture Compare channels
- Complementary output on channel 1



Basic timer

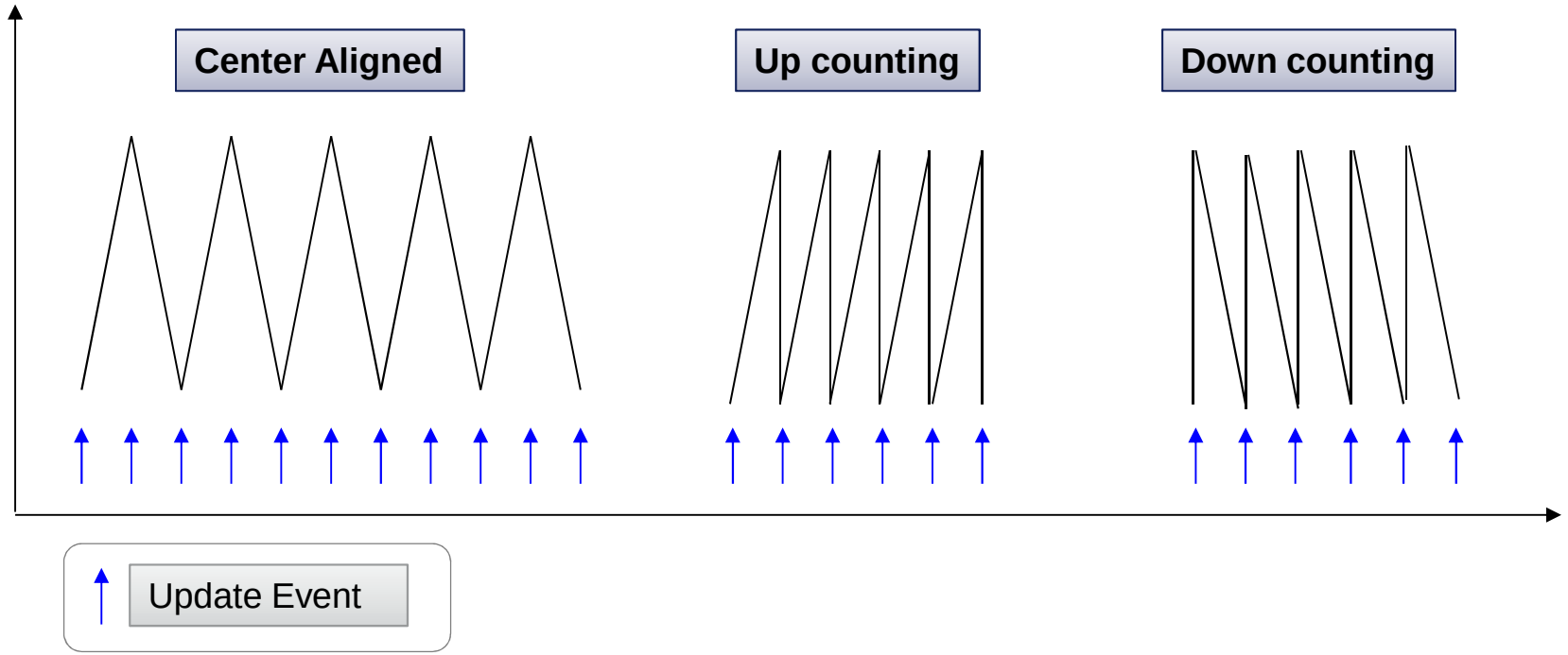
- No Capture Compare channels
- Counting period defined with autoreload register only
- Trigger output serves for trigger and time base generation purpose



TIM6/7

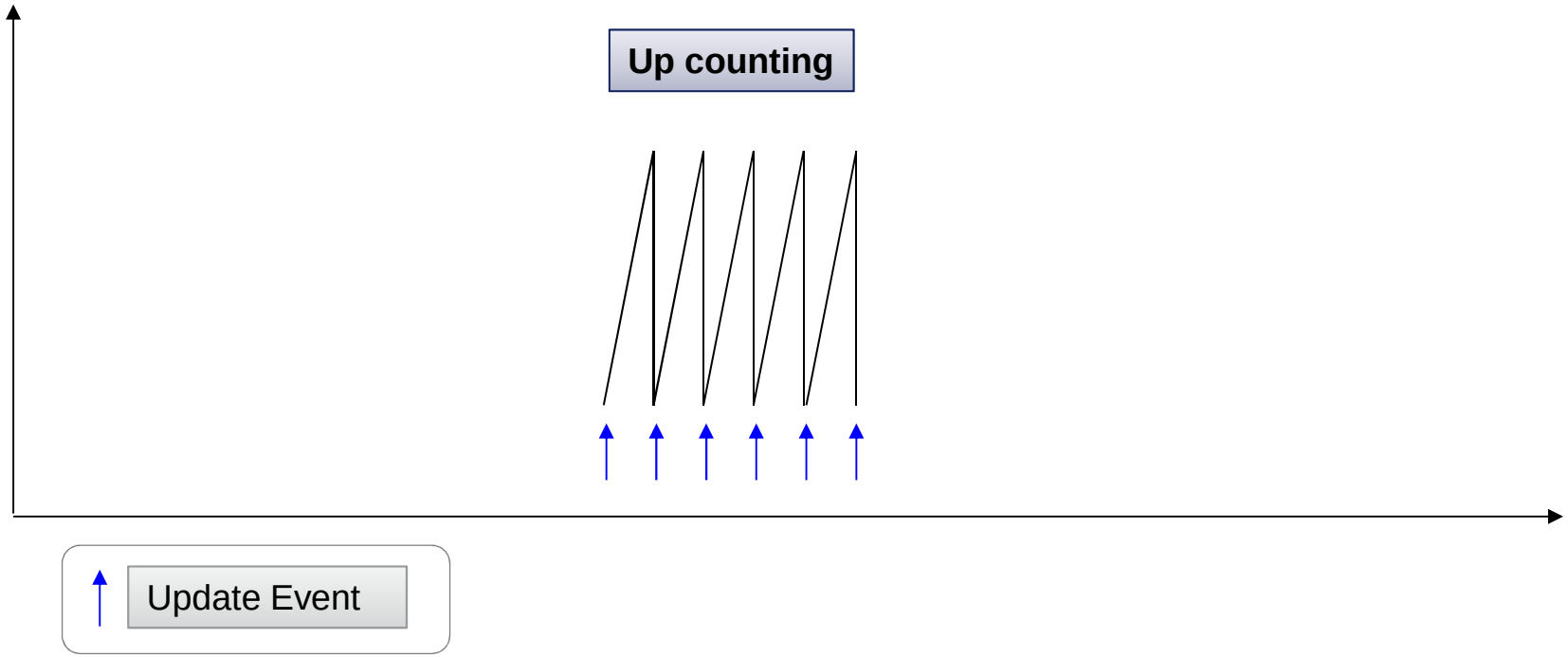
Counting Modes (1/2)

- Some timers have three counter modes:
  - Up counting mode
  - Down counting mode
  - Center-aligned mode



Counting Modes (2/2)

- One counting mode only for timers with less than 4 channels:
  - Up counting mode

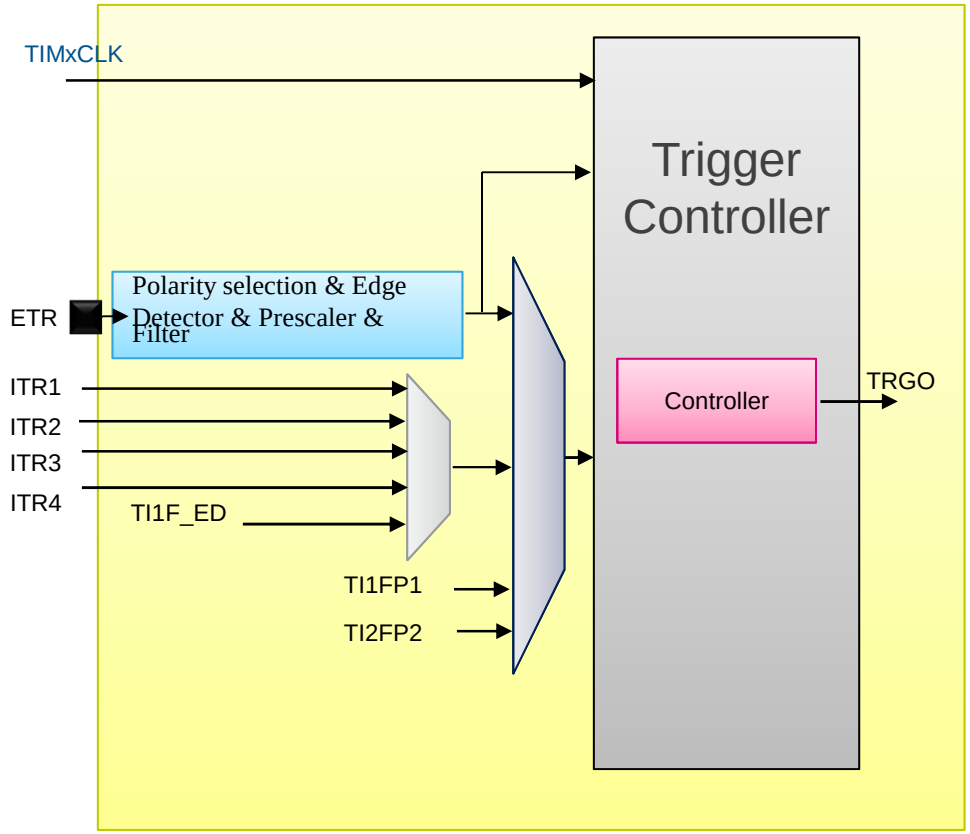


Update Event

- The content of the preload register is transferred into the shadow register
  - depends on the *Auto-reload Preload* feature if enabled or not
    - If enabled, at each Update Event the transfer occurs
    - If not enabled, the transfer occurs immediately
- The Update Event is generated
  - For each counter overflow/underflow
  - Through software, by setting the UG bit (Update Generation)
- The Update Event (UEV) request source can be configured to be
  - Next to counter overflow/underflow event
  - Nest to Counter overflow/underflow event plus the following events
    - Setting the UG bit by software
    - Trigger active edge detection (through the slave mode controller)

Counter Clock Selection

- Clock can be selected out of 8 sources
  - Internal clock TIMxCLK provided by the RCC
  - Internal trigger input 1 to 4:
    - ITR1 / ITR2 / ITR3 / ITR4
    - Using one timer as prescaler for another timer
  - External Capture Compare pins
    - Pin 1: TI1FP1 or TI1F_ED
    - Pin 2: TI2FP2
  - External pin ETR
    - Enable/Disable bit
    - Programable polarity
    - 4 Bits External Trigger Filter
    - External Trigger Prescaler:
      - Prescaler off
      - Division by 2
      - Division by 4
      - Division by 8
  - NB: TIM16/17/6/7 only have TIMxCLK

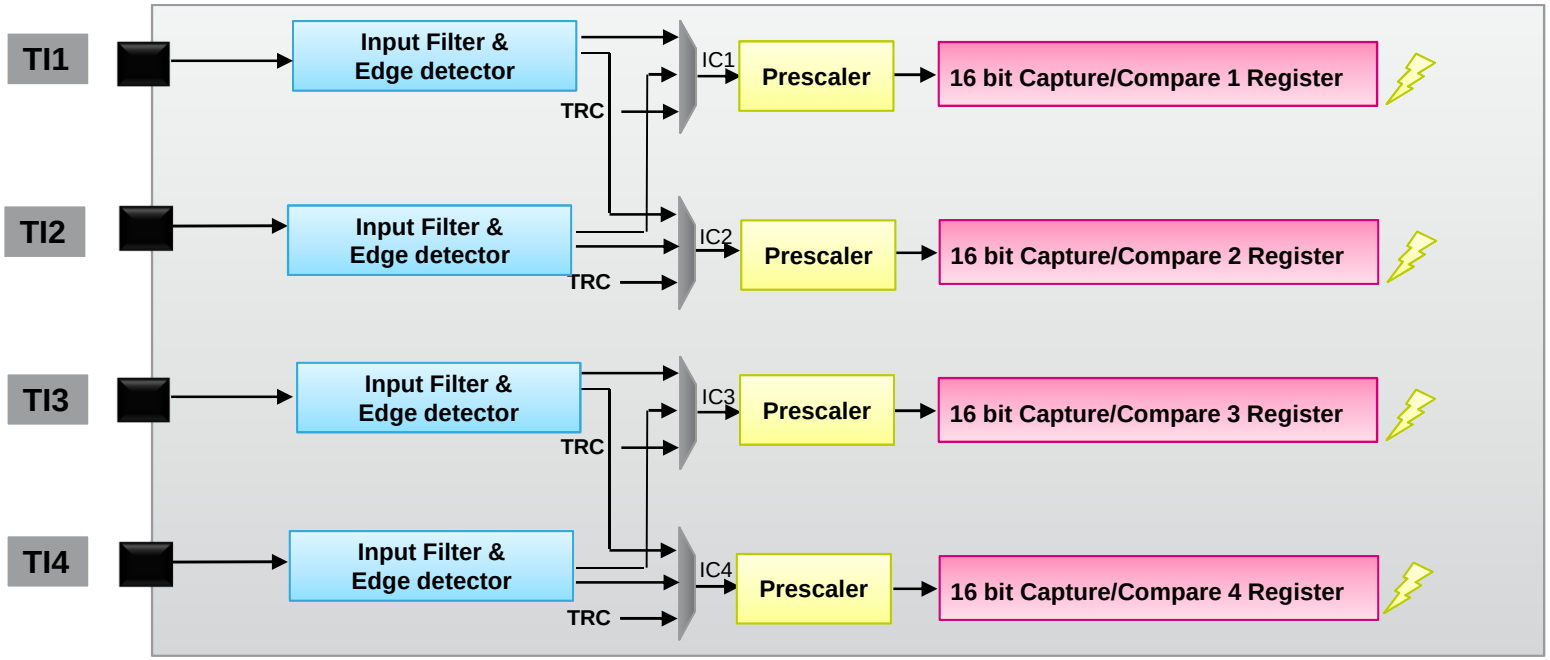


Capture Compare Array presentation

- Up to 4 channels
  - TIM2/3/4/5 have 4 channels
  - TIM15 have 2 channels
  - TIM16/17 have one channel
  - TIM6/7 have no channels
- Programmable bidirectional channels
  - Input direction: channel configured in **Capture** mode
  - Output direction: Channel configured in **Compare** mode
- Channel's main functional blocs
  - Capture/Compare register
  - Input stage for capture
    - 4-bit digital filter
    - Input Capture Prescaler
  - Output stage for Compare
    - Output control block

Input Capture Mode (1/2)

- Capture stage architecture (1 to 4 channels depending on timer)



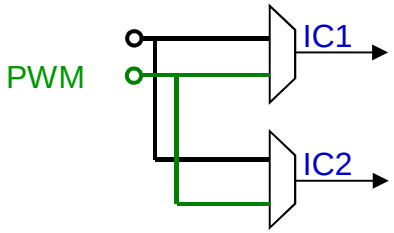
Input Capture Mode (2/2)

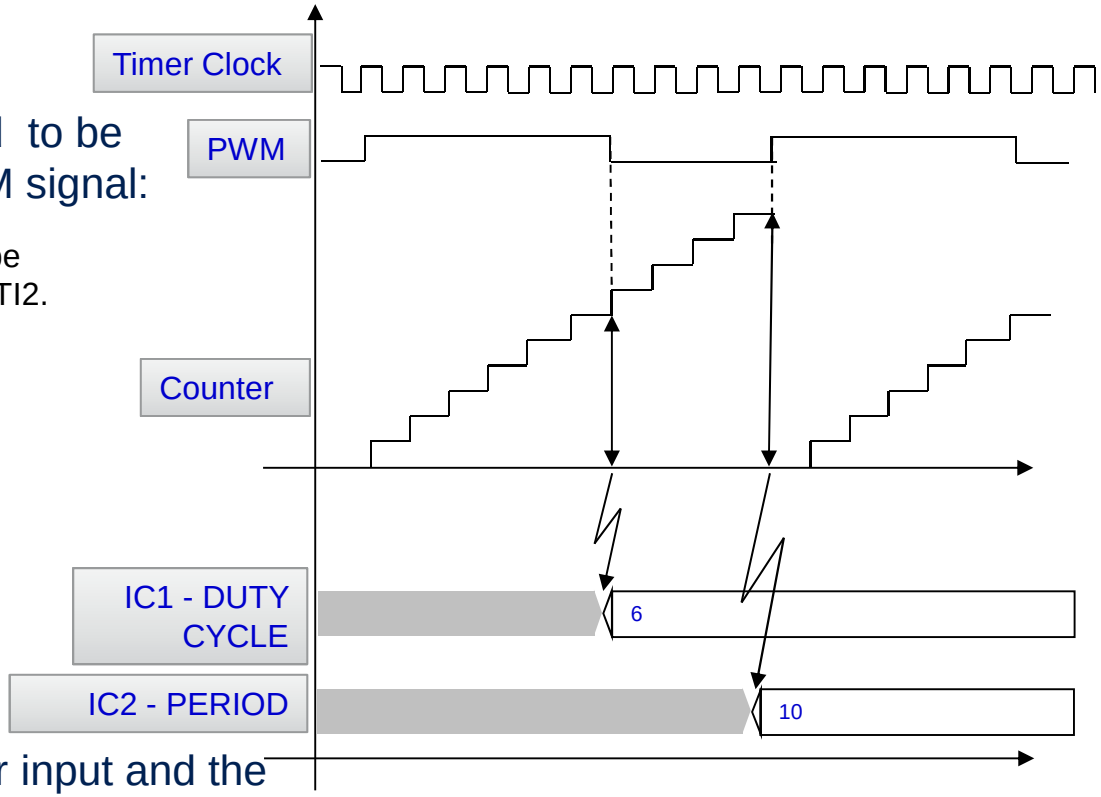
- Flexible mapping of TIx inputs to channels' inputs ICx
  - {TI1->IC1}, {TI1->IC2}, {TI2->IC1} and {TI2->IC2} are possible
- When an active Edge is detected on ICx input, the counter value is latched in the corresponding CCR register.
- When a Capture Event occurs, the corresponding CCXIF flag is set and an interrupt or a DMA request can be sent if they are enabled.
- An over-capture flag for over-capture signaling
  - Takes place when a Capture Event occurs while the CCxIF flag was already high

PWM Input Mode

- IC1 and IC2 must be configured to be connected together to the PWM signal:

⇨ IC1 and IC2 are redirected internally to be mapped to the same external pin TI1 or TI2.



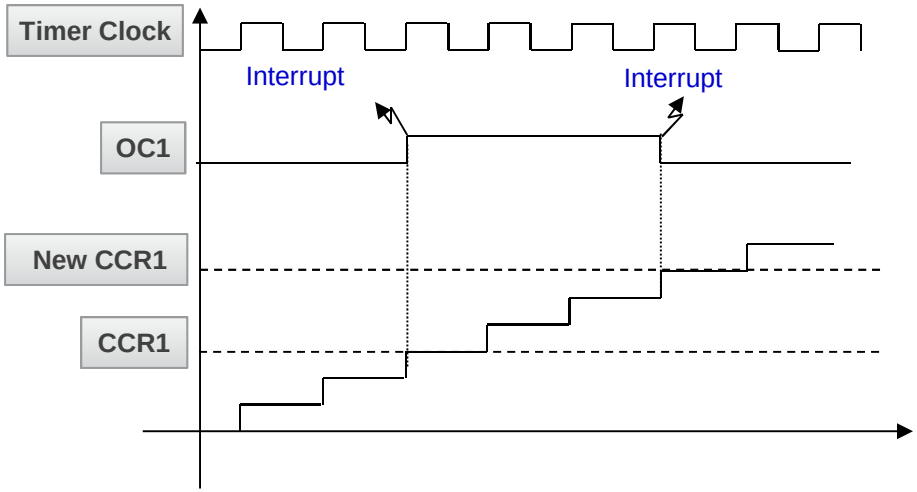


- IC1 and IC2 active edges must have opposite polarity.
- IC1 or IC2 is selected as trigger input and the slave mode controller is configured in reset mode.
- The PWM Input functionality enables the measurement of the period and the pulse width of an external waveform.

Output Compare Mode

- The Output Compare is used to control an output waveform or indicate when a period of time has elapsed.

- When a match is found between the capture/compare register and the counter:
  - The corresponding output pin is assigned to the programmable Mode, it can be:
    - Set
    - Reset
    - Toggle
    - Remain unchanged
  - Set a flag in the interrupt status register
  - Generates an interrupt if the corresponding interrupt mask is set
  - Send a DMA request if the corresponding enable bit is set

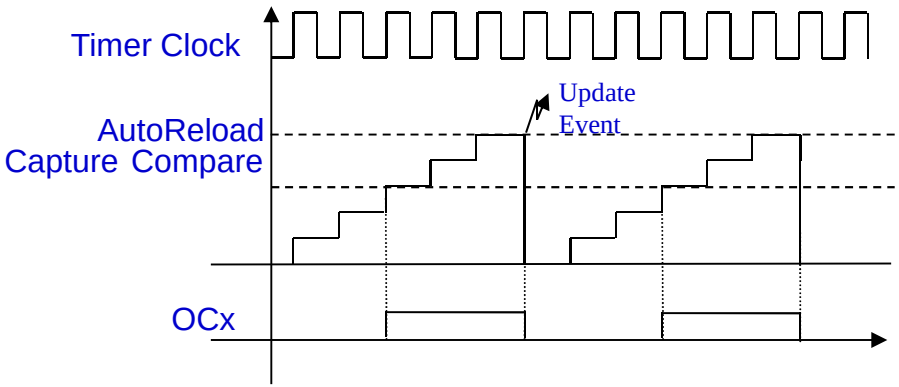


- The CCRx registers can be programmed with or without preload registers

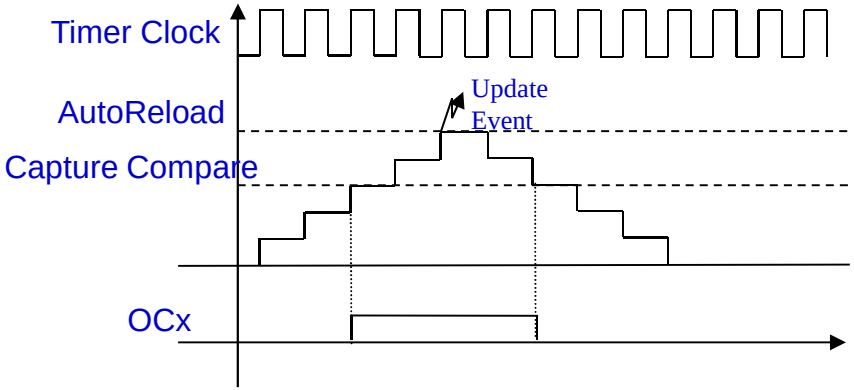
PWM Mode

- Available on all channels
- Two standard PWM mode available
  - PWM mode 1 (ouput active when counter > compare)
  - PWM mode 2 (ouput active when counter < compare)
  - Each PWM mode behavior (waveform shape) depends on the counting direction

Edge-aligned Mode



Center-aligned Mode



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TIM1/8 TIM2/3/4/5 TIM15 TIM16/17

Channels Coupling (1/2)

- Two coupling schemes:
  - Adjacent channels coupling:
    - Channel1 and Channel2 coupling
    - Channel3 and channel4 coupling
  - Enhanced channels coupling (feature used for Motor Control applications)
    - Channel5 and Channel1
    - Channel5 and Channel2
    - Channel5 and Channel3
- Flexible coupling mechanism on adjacent channels
  - Channels coupling output can be directed to one channel or to both of them
- Generated Waveforms' shape
  - Frequency control through TIMx_ARR register value
  - Phase-shift (delay) control through one of the two channels' TIMx_CCR register
  - Pulse-length (duty-cycle) control through the second channels' TIMx_CCR register

Channels Coupling (2/2)

- Available PWM modes
  - Each channel among the first four channels can be configured in one of the following PWM modes
  - Asymmetric and Combined PWM modes are applicable on coupled channels only

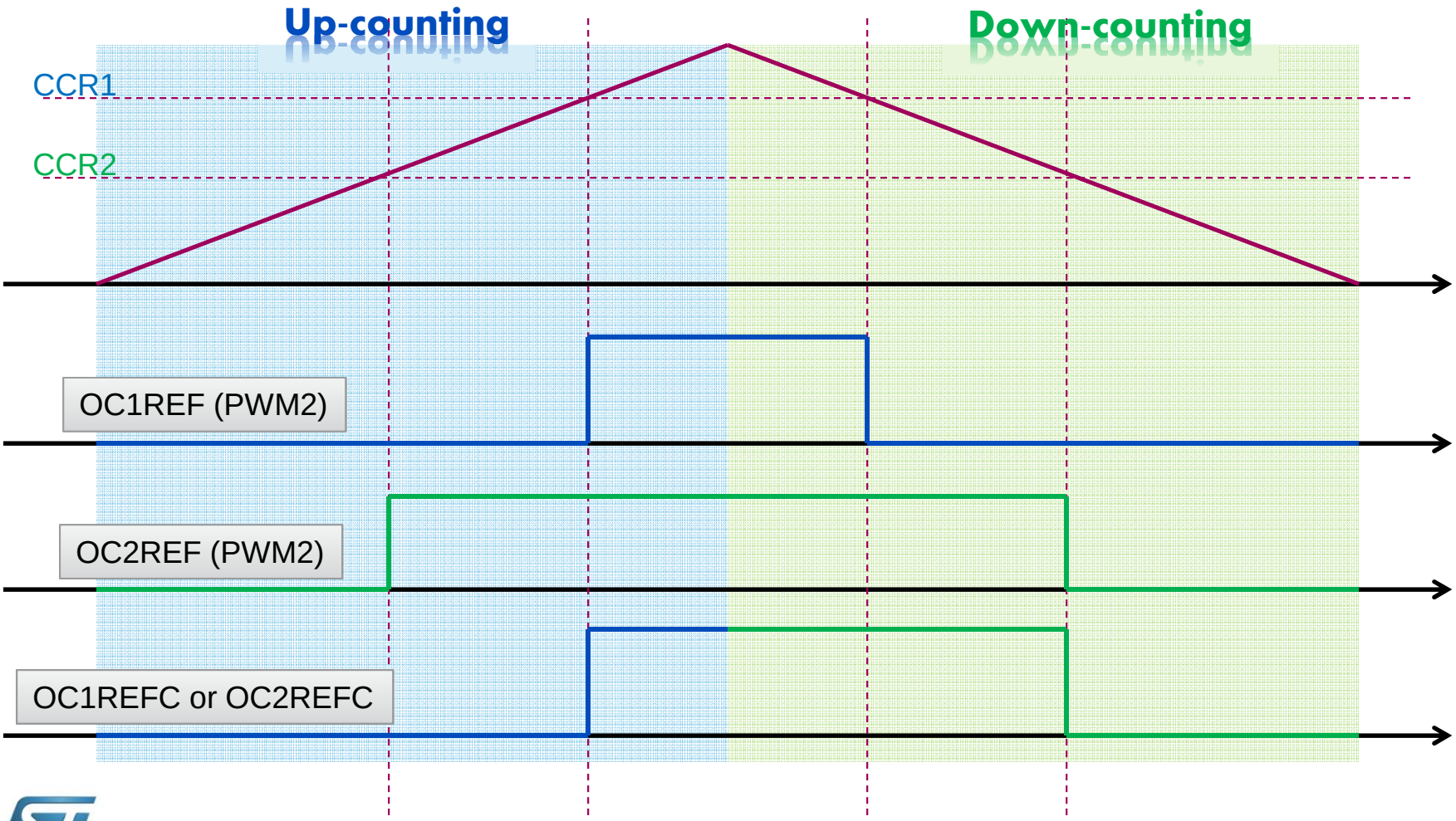
	PWM mode 1	PWM mode 2
Independent	OCxM[3:0] = 4b'0110'	OCxM[3:0] = 4b'0111'
Asymmetric	OCxM[3:0] = 4b'1110'	OCxM[3:0] = 4b'1111'
Combined	OCxM[3:0] = 4b'1100'	OCxM[3:0] = 4b'1101'

Coupling between channels is activated

TIM1/8 TIM2/3/4/5 TIM15

Asymmetric PWM mode (1/3)

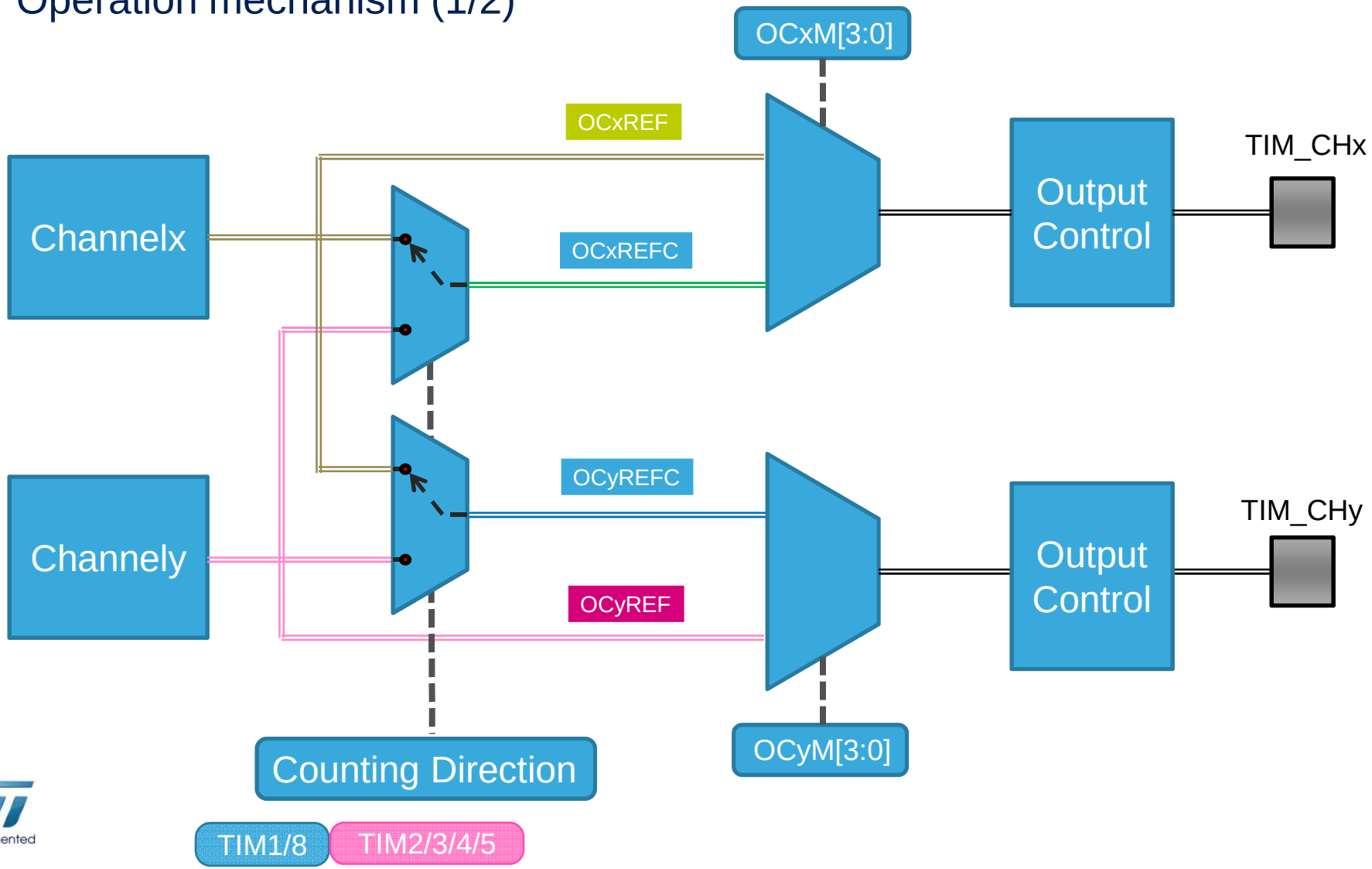
- Output waveform shape



TIM1/8 TIM2/3/4/5

Asymmetric PWM mode (2/3)

- Operation mechanism (1/2)

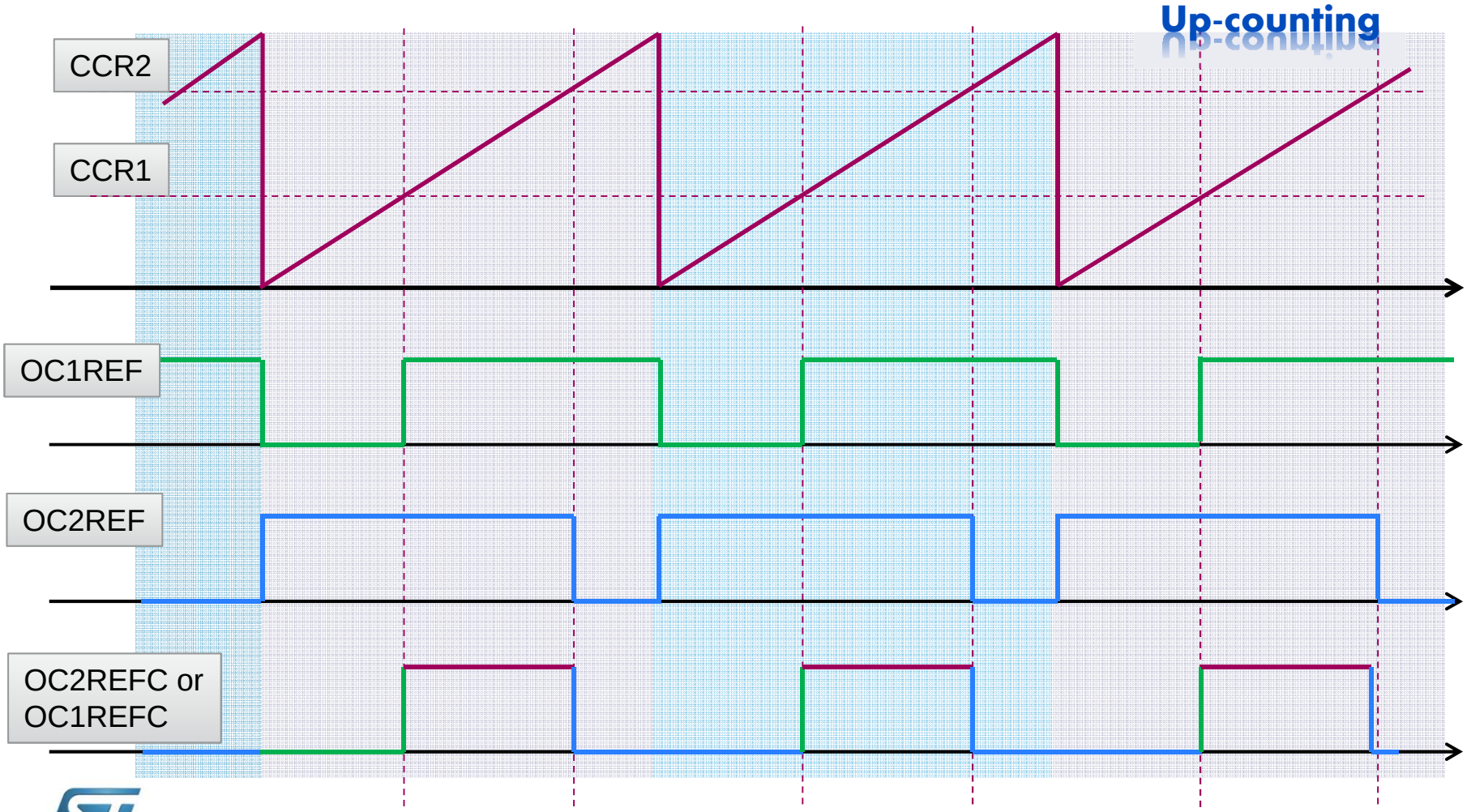


Asymmetric PWM mode (3/3)

- Operation mechanism (2/2)
  - The counting direction selects which channel output to be directed to OCxREFC
  - Coupled channel has to be configured in the same PWM mode
- Center-aligned counting mode required
  - Asymmetric mode is **effective** only when the timer is configured to count in **center-aligned** mode
- Available on the following channel couples:
  - (Channel1, Channel2)
  - (Channel3, Channel4)
- Two Asymmetric PWM mode are available
  - Asymmetric PWM1 mode
  - Asymmetric PWM2 mode

Combined PWM mode (1/5)

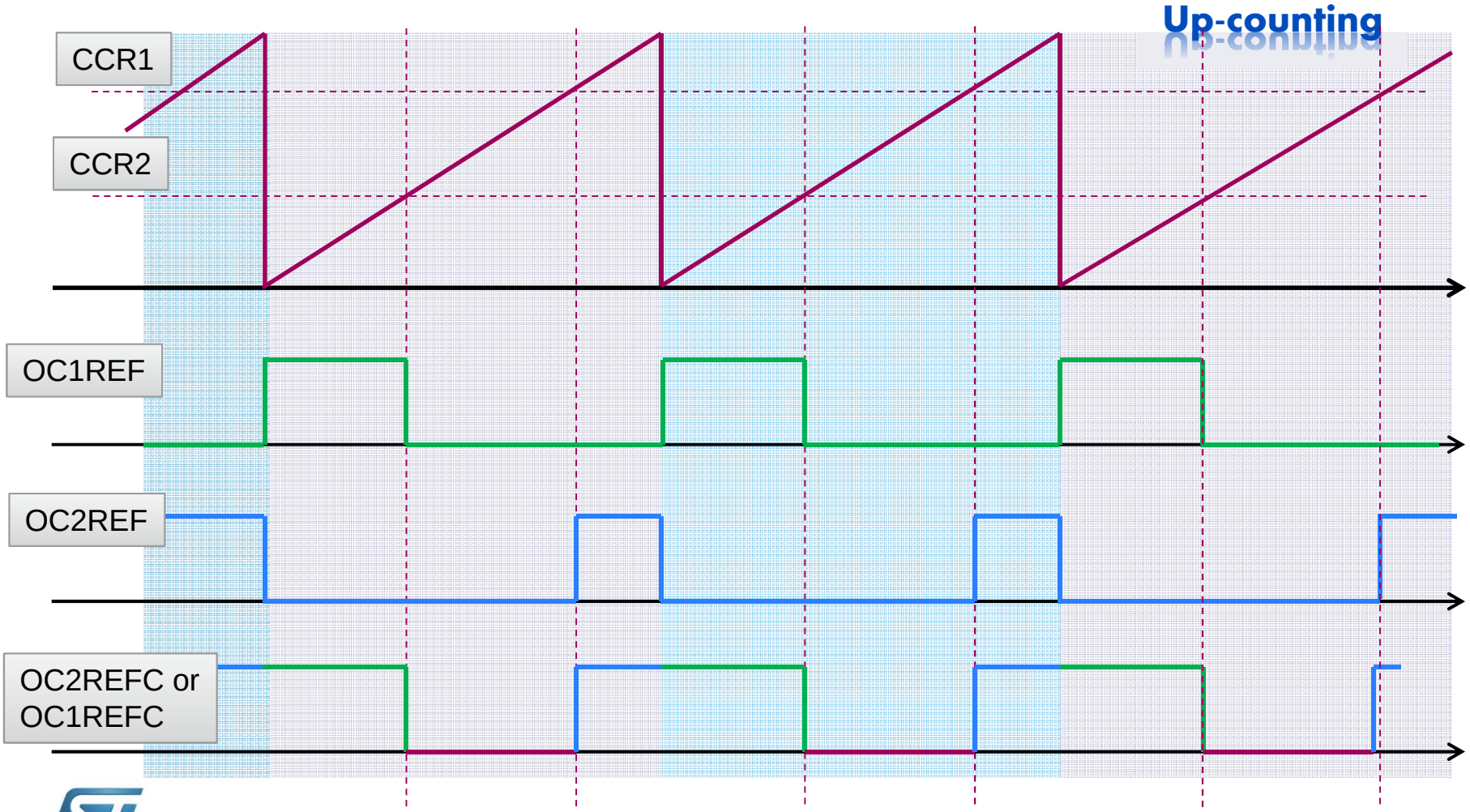
- Output waveform shape (Logical And)



TIM1/8 TIM2/3/4/5 TIM15

Combined PWM mode (2/5)

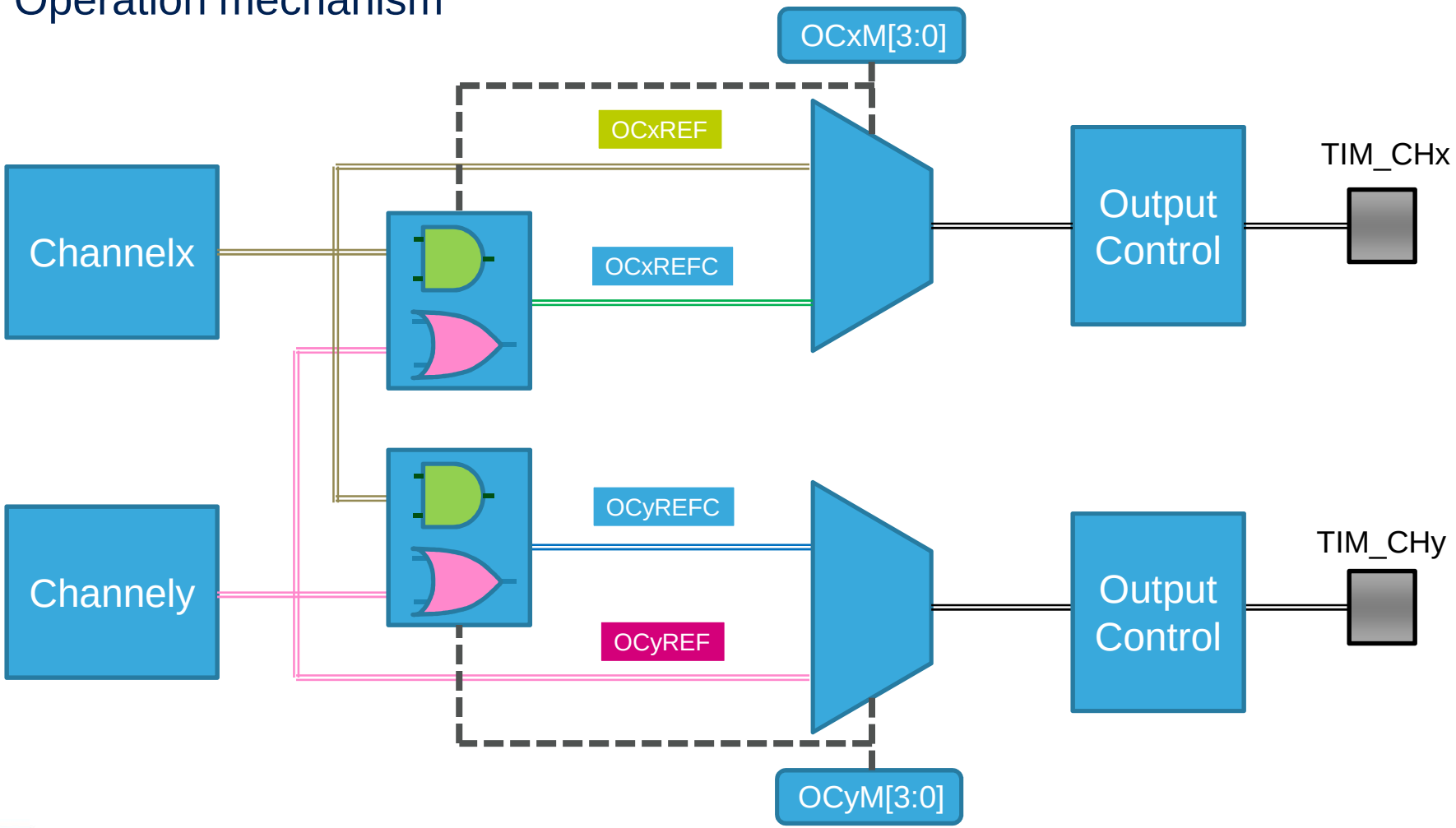
- Output waveform shape (Logical Or)



TIM1/8 TIM2/3/4/5 TIM15

Combined PWM mode (3/5)

- Operation mechanism



Combined PWM mode (4/5)

- Two logical operators coupling modes:
  - Logical **And**
  - Logical **Or**
- Two Combined PWM mode are available
  - Combined PWM1 mode
  - Combined PWM2 mode
- Different PWM mode on each channel
  - In order to get the desired output, the two coupled channels has to be configured with different PWM modes: PWM1 and PWM2
  - If the same PWM mode is configured on both channels, the output signal waveform is similar to one of the two channels waveforms depending on the Logical Operator applied

Combined PWM mode (5/5)

- Configuration sequence
  - Configure the two coupled channels on different PWM modes
  - Configure one channel or both coupled channels to output a logical combination of the channels' waveforms
- Counting mode independent:
  - Acts on Edge-aligned counting mode
  - Acts on Center-aligned counting mode
- Available on the following channel couples:
  - (Channel1, Channel2)
  - (Channel3, Channel4)

Channels 5&6 features

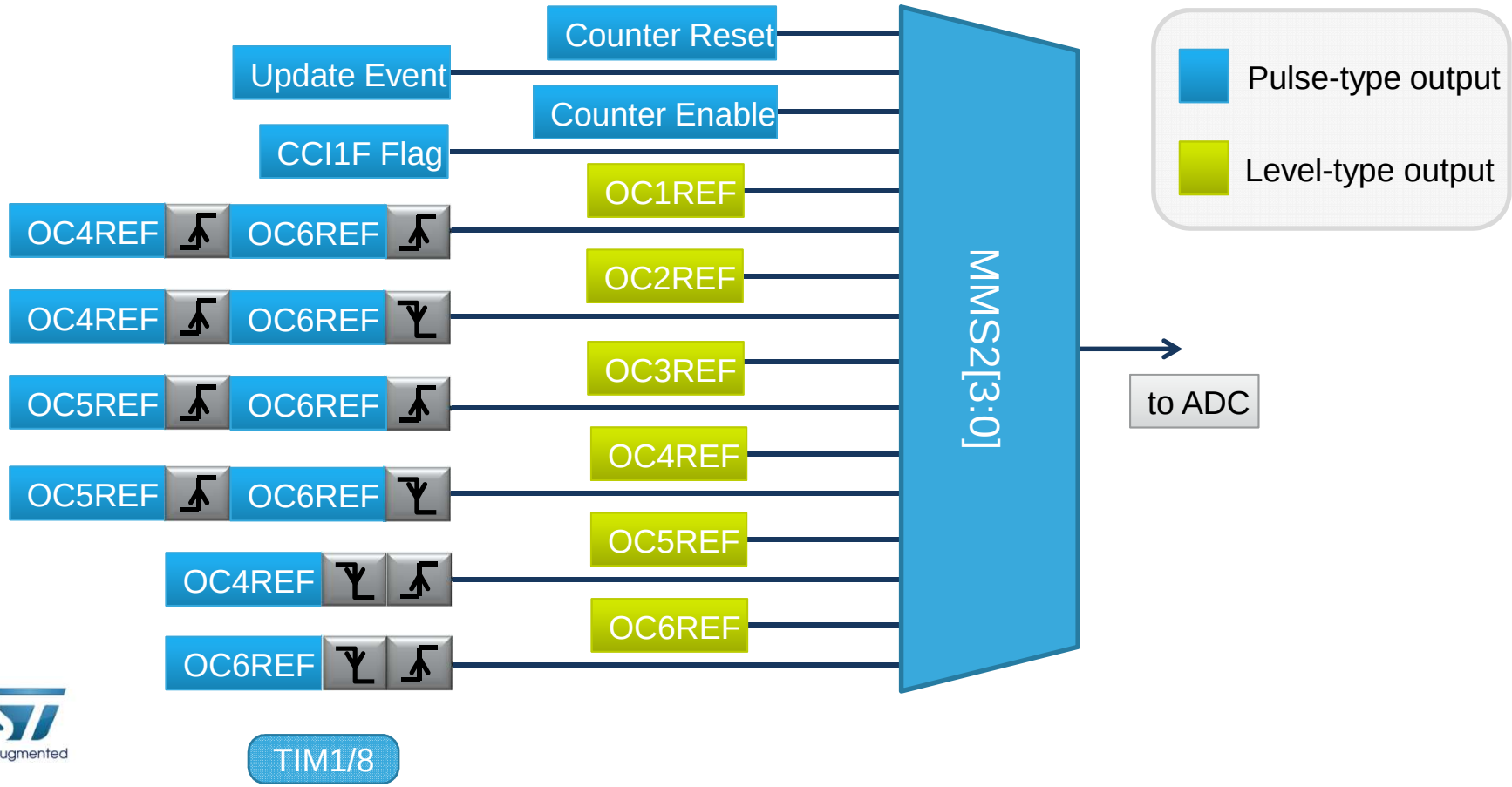
(Advanced control timers only)

- Channels 5&6 characteristics:
  - Internal channels
    - Not wired to GPIOs
    - Used within the Timer itself for complex waveform generation
    - Routed to the ADC triggering logic (via Timer's TRGO output)
  - Compare-and-PWM-modes-only channels
    - No capture modes
    - No DMA channels nor Interrupt request lines
- Channel 5&6 use cases:
  - Can be used to generate more complex waveforms when combined with other channels (applicable for Channel5 only)
  - Can be used to trigger ADC conversion (many triggering scenarios)
- Typical use case
  - Additional features for PWM distortion and additional ADC triggers

Enhanced Triggering mechanism

(Advanced control timers only)

- Additional set of triggers dedicated for ADC
  - Outputted on the new (second) trigger output TRGO2
  - Controlled through the new bit-field MMS2[3:0]



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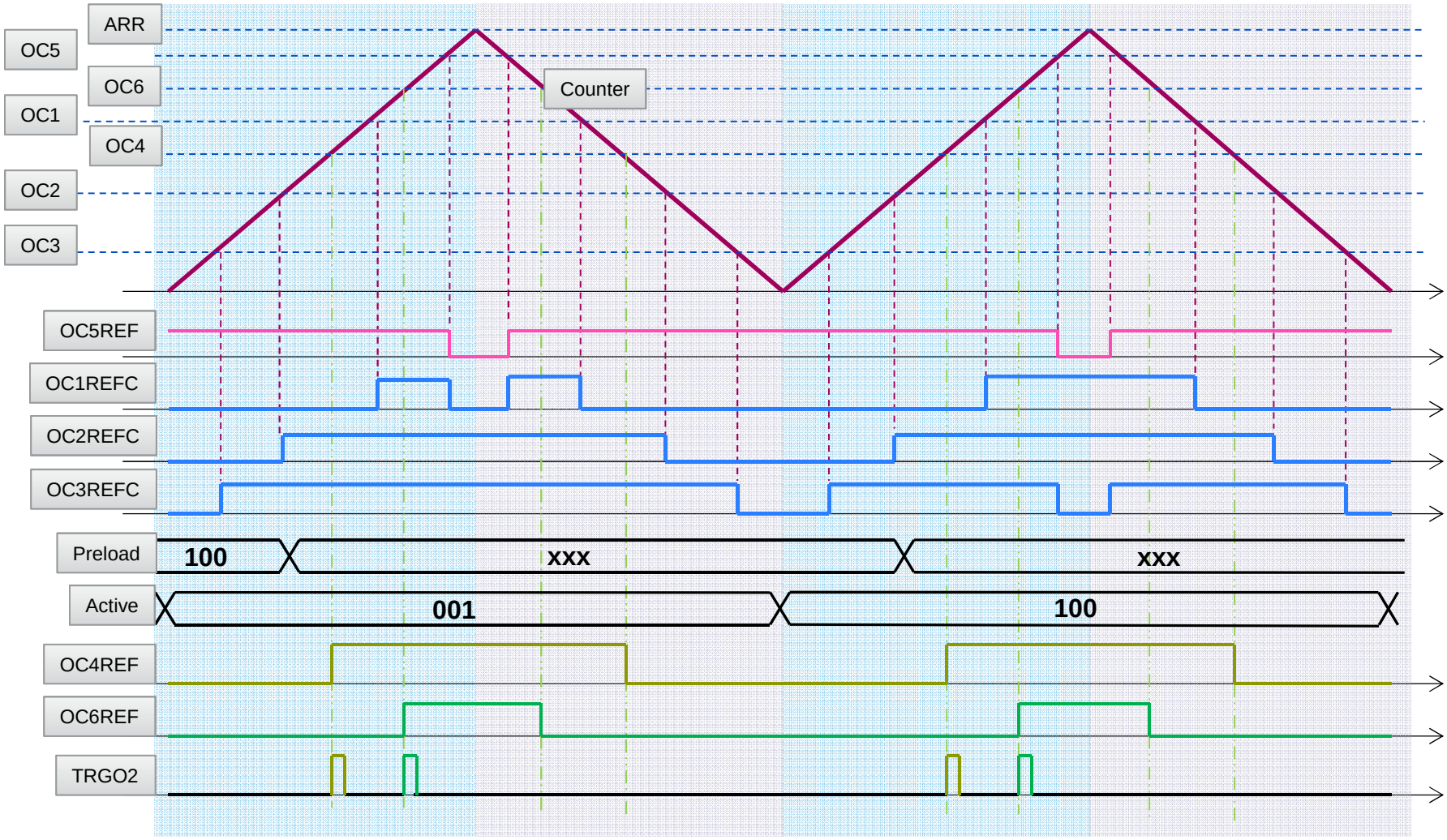
Combined 3-phase PWM mode (1/3)

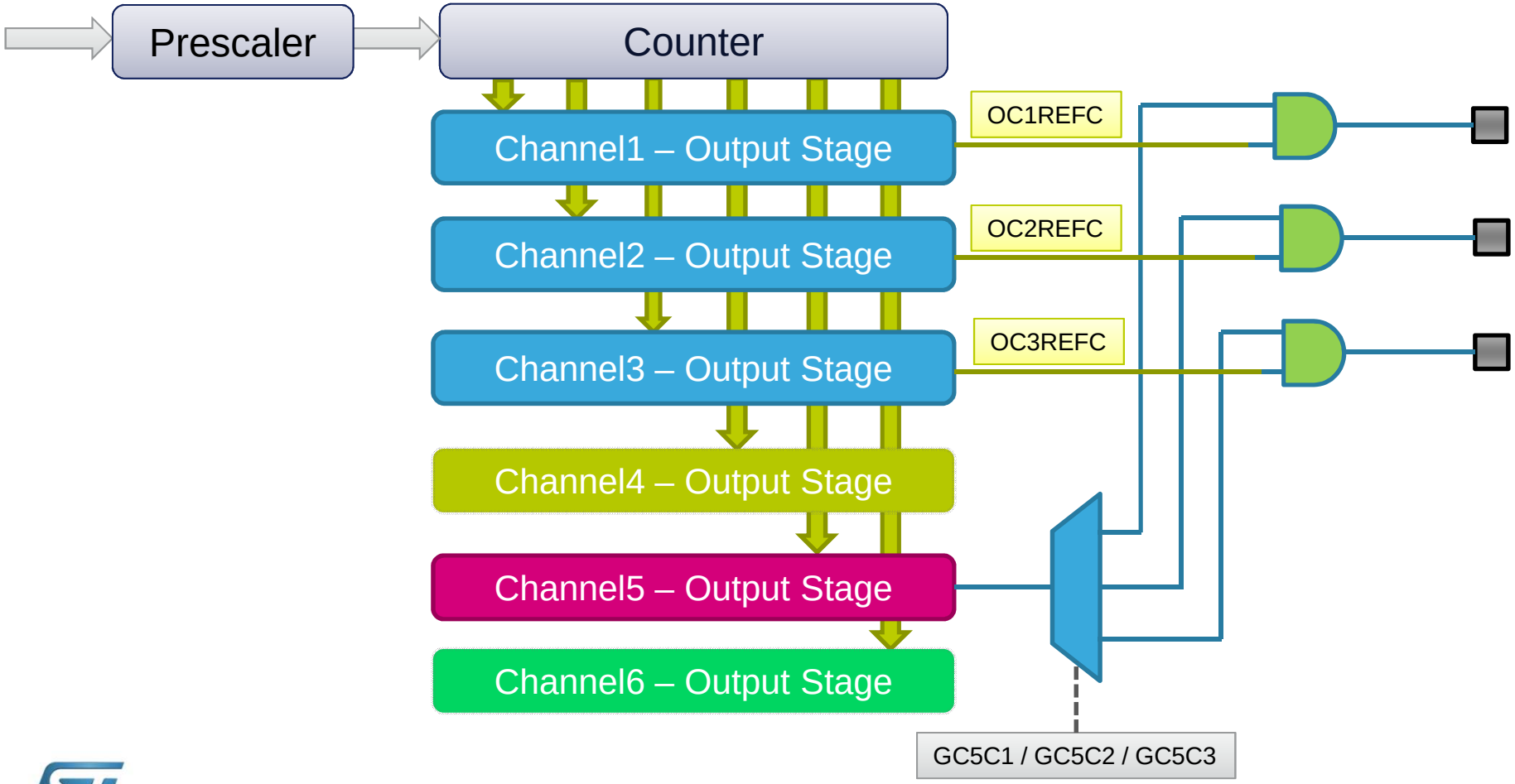
(Advanced control timers only)



Combined 3-phase PWM mode (2/3)

(Advanced control timers only)

- Operation mechanism



Combined 3-phase PWM mode (3/3)

(Advanced control timers only)

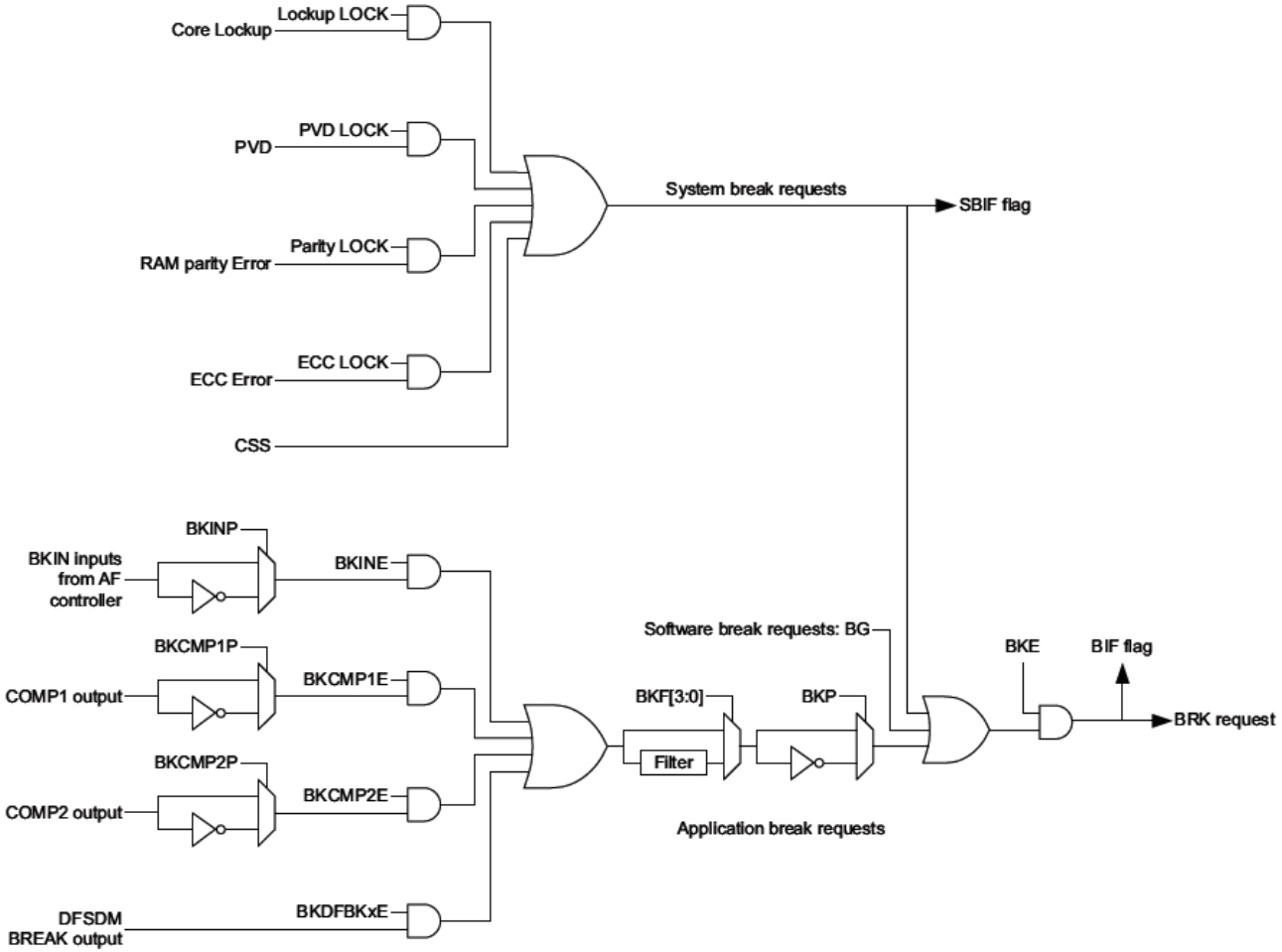
- Waveforms generation on up to three channels
  - Based on coupling Channel5's output with others channels
    - Channel1
    - Channel2
    - Channel3
- Dedicated for Motor Control application
  - Used by ST's patented Single-shunt current reading application
  - Can reduce CPU load by 5-10% compared to current implementation on F1/F2/F4 families
  - Frees many MCU resources (DMA channels, Interrupt request lines)

Break inputs

- The break inputs allow to shutdown by hardware the PWM outputs for safety purposes
- Up to two break input sources
  - Break input 1
    - Idle State programming
    - Has the highest priority over Break inputs
    - Multiplexed with internal break signals
      - CSS, SRAM parity error, Comparators outputs, PVD interrupt, Cortex M4 lockup
    - Built with a digital filter with a flexible set of sampling periods
    - Asynchronous functioning (unless the filter is enabled)
    - Typical use case: Over-voltage protection handling
  - Break input 2 (only on TIM1/TIM8)
    - No Idle State programming
    - Lower priority compared to Break input 1 (legacy one)
    - Built with a digital filter with a flexible set of sampling periods
    - Typical use case: Over-current protection handling

Break input selection

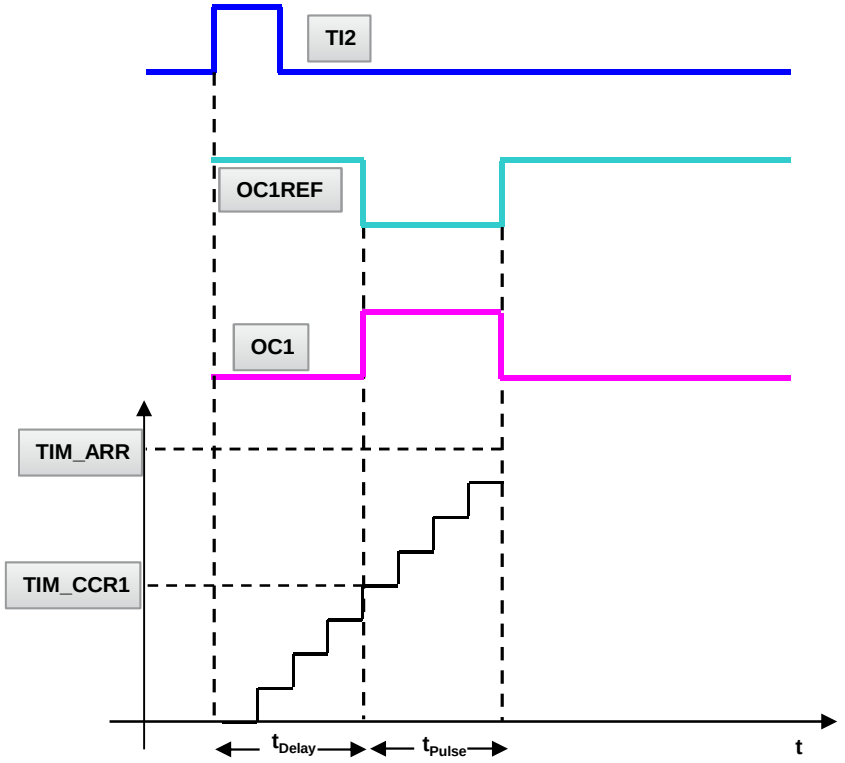
- Break request from comparators and DFSDM are controlled using TIMx_OR2 register



TIM1/8 TIM15 TIM16/17

One Pulse Mode (1/2)

- One Pulse Mode (OPM) is a particular case of Output Compare mode
- It allows the counter to be started in response to a stimulus and to generate a pulse
  - With a programmable length
  - After a programmable delay
- There are two One Pulse Mode waveforms selectable by software:
  - Single Pulse
  - Repetitive Pulse



One Pulse Mode (2/2)

Exercise:

How to configure One Pulse Mode to generate a repetitive Pulse in response to a stimulus ?

One Pulse Mode configuration steps

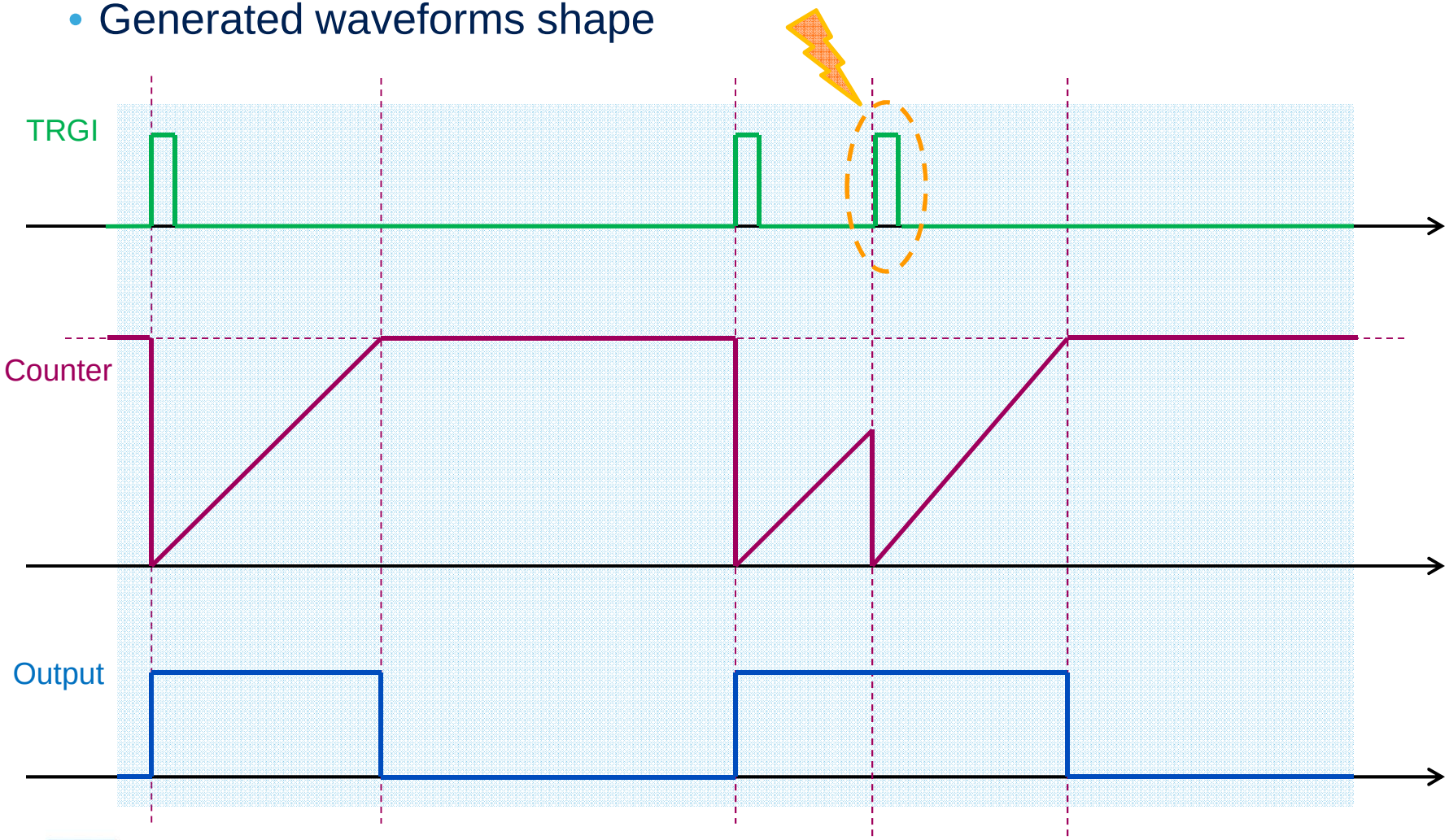
1. Input Capture Module Configuration:
   - i. Map TIxFPx on the corresponding TIx.
   - ii. TIxFPx Polarity configuration.
   - iii. TIxFPx Configuration as trigger input.
   - iv. TIxFPx configuration to start the counter (Trigger mode)

2. Output Compare Module Configuration:
   - i. OCx configuration to generate the corresponding waveform.
   - ii. OCx Polarity configuration.
   - iii. t_{Delay} and t_{Pulse} definition.

3. **One Pulse Module Selection: Set or Reset the corresponding bit (OPM) in the Configuration register (CR1).**

Retriggerable One Pulse Mode (1/2)

- Generated waveforms shape



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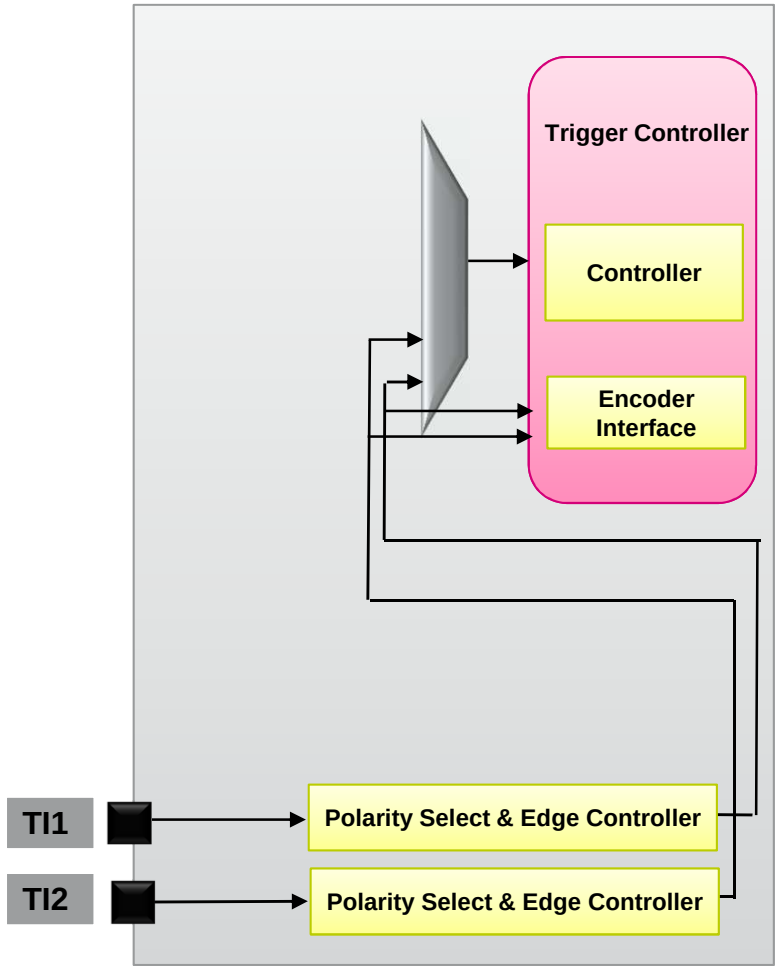
TIM1/8 TIM2/3/4/5 TIM15

Retriggerable One Pulse Mode (2/2)

- Available on Channel 1, 2, 3 and 4
- Different from the existing One Pulse mode:
  - The outputted pulse starts as soon as a trigger active edge is detected
  - The pulse length is extended if a new active edge is detected
- Pulse length is set using the ARR register
  - For Up-counting mode, CCRx register has to be set to zero
  - For Down-counting mode, CCRx register has to be set to ARR value
- Configuration sequence
  - Set the timer to **slave** mode: the ***Combined Reset+Trigger*** mode **shall** be used
  - Select the Retriggerable One Pulse mode through the OCxM[3:0] bit field
    - Retriggerable OPM mode 1
    - Retriggerable OPM mode 2

Encoder Interface (1/2)

- Encoders are used to measure position and speed of mobile systems (either linear or angular)
- The encoder interface mode acts as an external clock with direction selection
- Encoders and Microcontroller connection example:
  - A can be connected directly to the MCU without external interface logic.
  - The third encoder output which indicates the mechanical zero position, may be connected to an external interrupt and trigger a counter reset.
- Encoder enhancement
  - A copy of the Update Interrupt Flag (UIF) is copied into bit 31 of the counter register
  - Simultaneous read of the Counter value and the UIF flag : Simplify the position determination



Encoder Interface (2/2)

Exercise:

How to configure the Encoder interface to detect the rotation direction of a motion system?

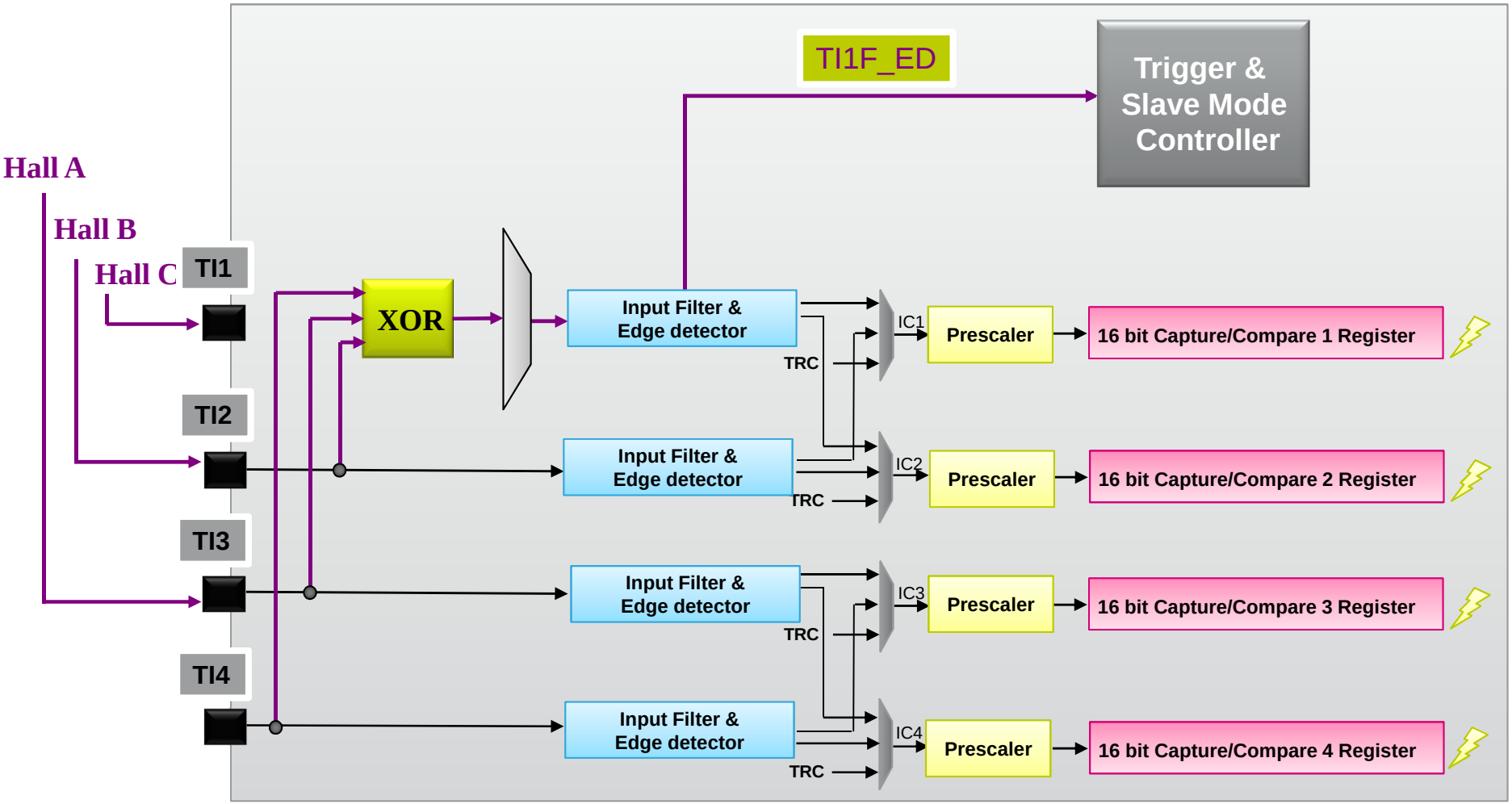
Encoder interface configuration steps:

1. Select the active edges: example counting on TI1 and TI2.
2. Select the polarity of each input: example TI1 and TI2 polarity not inverted.
3. Select the corresponding Encoder Mode.
4. Enable the counter.

Encoder Mode enhancement

- Two Timers can share the same Quadrature Encoder output signals
  - TIM2 IC1 (*respectively TIM2 IC2*) is connected to TIM15 IC1 (*respectively TIM15 IC2*)
  - TIM3 IC1 (*respectively TIM3 IC2*) is connected to TIM15 IC1 (*respectively TIM15 IC2*)
  - TIM4 IC1 (*respectively TIM4 IC2*) is connected to TIM15 IC1 (*respectively TIM15 IC2*)
- Configuration
  - Using ENCODER_MODE[1:0] bit field within the TIM15_OR1 register
- Use case
  - Used with M/T technique for estimating Velocity and Acceleration for wide-range of velocity values (especially for low velocity values)

Hall sensor Interface (1/2)

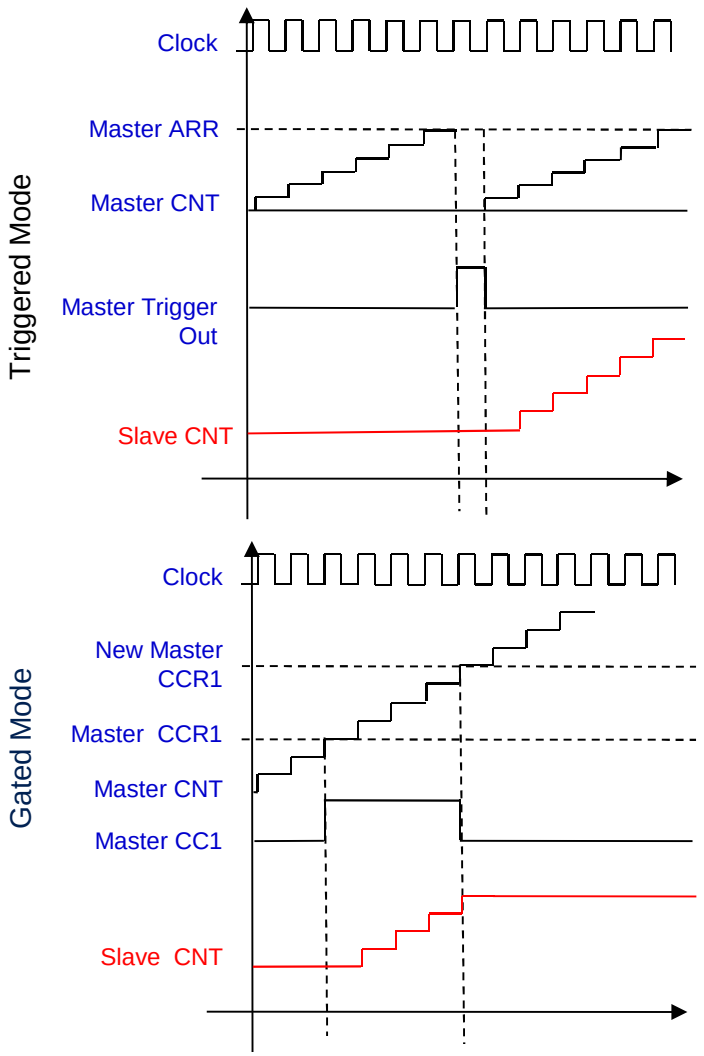


Hall sensor Interface (2/2)

- Hall sensors are used for:
  - Speed detection
  - Position sensor
  - Brushless DC Motor Sensor
- How to configure the TIM to interface with a Hall sensor?
  - Select the hall inputs for TI1: TI1S bit in the CR2 register
  - The slave mode controller is configured in reset mode
  - TI1F_ED is used as input trigger
- To measure a motor speed:
  - Use the Capture/Compare Channel 1 in Input Capture Mode
  - The Capture Signal is the TRC signal
  - The captured value which correspond to the time elapsed between 2 changes on the inputs, gives an information about the motor speed

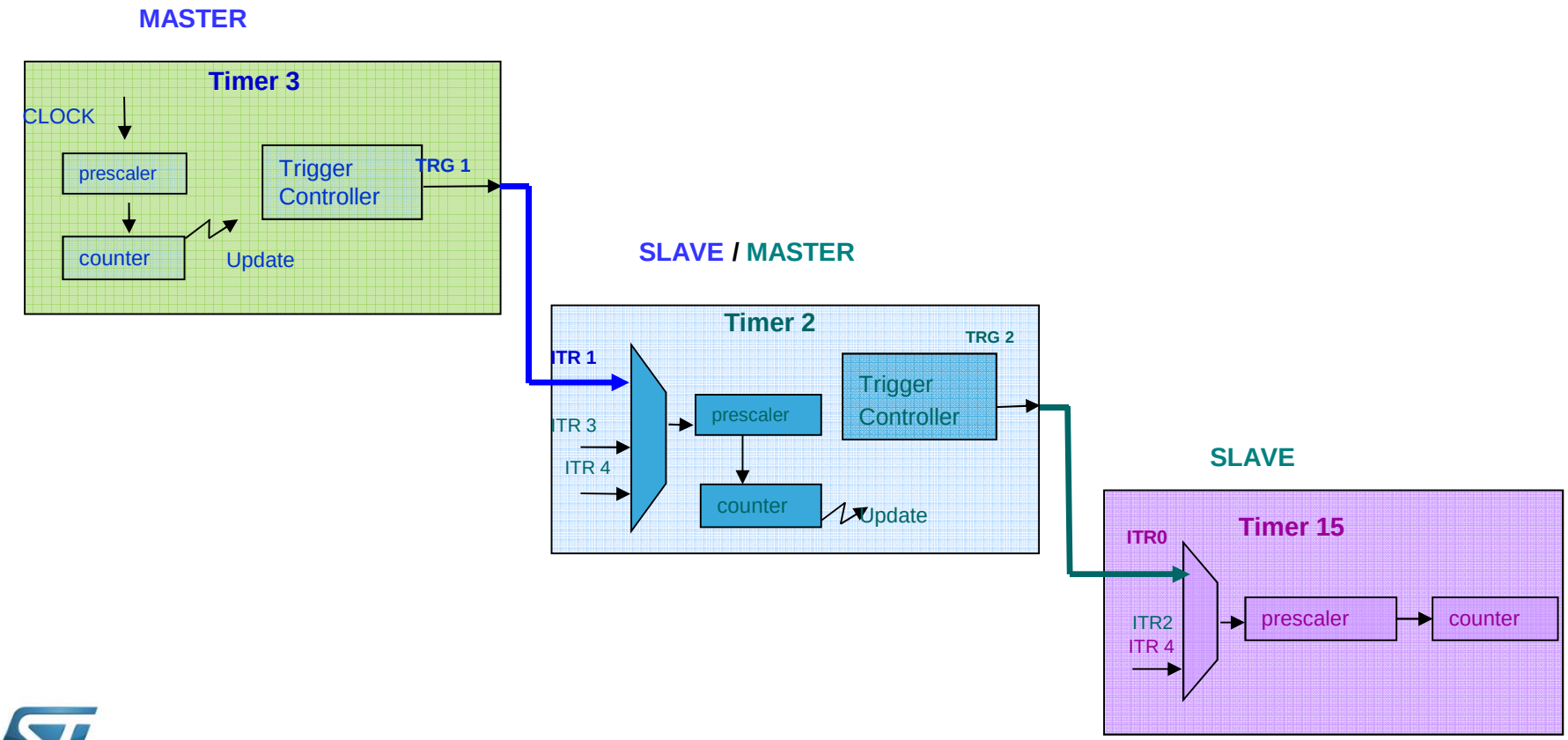
Synchronization Mode Configuration

- The Trigger Output can be controlled on:
  - Counter reset
  - Counter enable
  - Update event
  - OC1 / OC1Ref / OC2Ref / OC3Ref / OC4Ref signals
- The slave timer can be controlled in two modes:
  - Triggered mode : only the start of the counter is controlled
  - Gated Mode: Both start and stop of the counter are controlled
  - Reset Mode - Rising edge of the selected trigger input (TRGI) reinitializes the counter
  - Combined reset + trigger Mode (for re-trigerrable one pulse mode)
- NB: TIM16/17 OC outputs can be used for synchronization



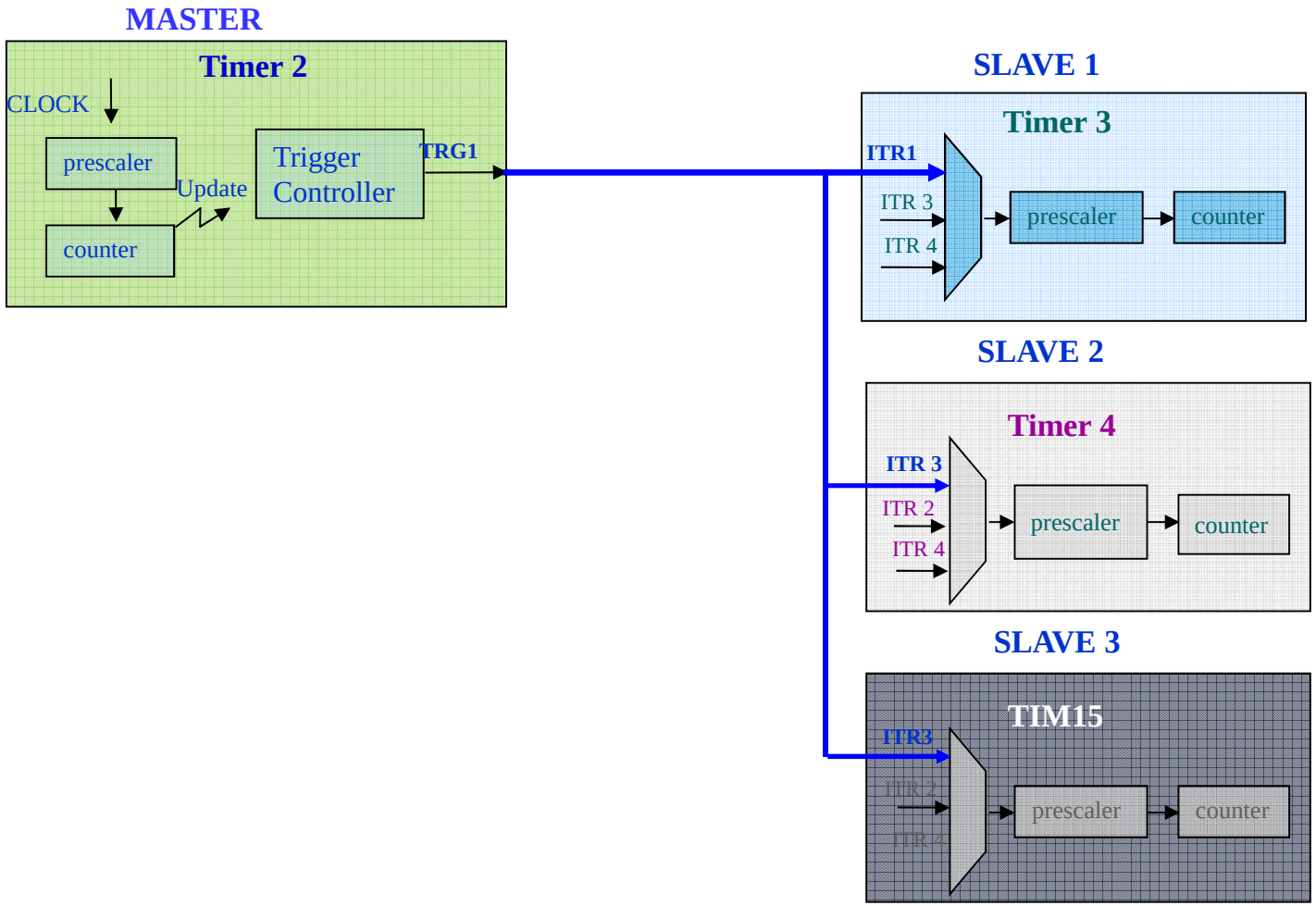
Synchronization: Configuration examples (1/3)

- Cascade mode:
  - TIM3 used as master timer for TIM2
  - TIM2 configured as TIM3 slave, and master for TIM15



Synchronization: Configuration examples (2/3)

- One Master several slaves: TIM2 used as master for TIM3, TIM4 and TIM15



Synchronization: Configuration examples (3/3)

- Timers and external trigger synchronization
  - TIM2, TIM3 and TIM4 are slaves for an external signal connected to respective Timers inputs